

# Low-Voltage NAND Flash Memory Without Hardware Modifications

Mastooreh Salajegheh<sup>1</sup>  
Qualcomm Research  
negin@qti.qualcomm.com

Kevin Skadron  
University of Virginia  
skadron@virginia.edu

Mircea Stan  
University of Virginia  
mircea@virginia.edu

## Abstract

While NAND flash memory has become the primary storage for pervasive computing, its power consumption is still higher than desirable for battery-powered devices. To reduce the power consumption of flash memory, we propose to operate NAND flash at voltages lower than required by the specifications. This paper shows that 1) the reliability of MLC (Multi-Level Cell) flash memory at sub-threshold voltages are affected minimally and 2) repeating a *write* operation in case it fails the first time can remedy the errors efficiently. This new result is consistent with previous studies on NOR SLC flash memory [2]. Our experiments have shown that MLC flash chips can be greatly underpowered and still be operated with an extremely small effect on their error rates. For example, an MLC flash memory chip, with minimum voltage requirement of 2.7 V, can be operated at a fixed 1.6 V, with an error rate of 0.014%. As the result of this low operating voltage, the energy consumption will drop from 118 J to 58 J (103% improvement).

## NAND Flash Behavior at Low Voltages

We propose to examine the behavior of MLC NAND flash memory under fixed low voltages. We have measured the error rate of a MLC flash memory in a voltage range of 1.3 V–3.6 V. We define *write* errors as the number of bit differences in the data intended to be stored in flash, compared to the value read from the flash. The result (Figure 1) indicates that the change in *write* error rate is negligible even if the voltage is as low as 1.7V, even though the minimum required voltage is specified as 2.7V by the manufacturer.

While the voltage level affects flash writes, our experiments show that *read* and *erase* operations are not affected visibly. In another set of experiments, we programmed one page of flash memory at high voltage, and then read/erase it at lower voltages. The introduced error

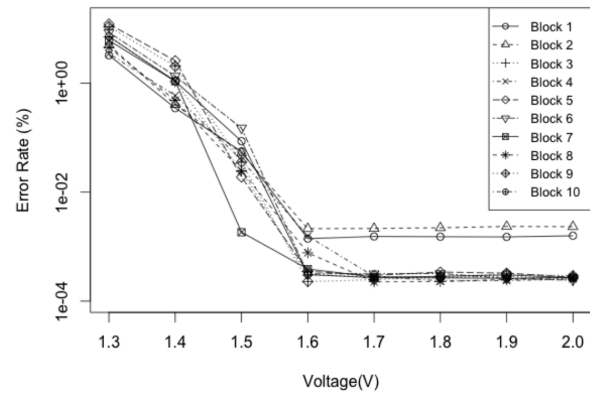


Figure 1: Error Rate decreases as the voltage increases. For this specific MLC flash memory, the change in error rate is negligible even if the voltage is as low as 1.7 V (minimum of 2.7 V required by the manufacturer).

was negligible.

Aside from voltage level, memory address plays a role in the error rate. Due to process variation, different pages of flash memory have different resistance and as a result some pages are more error prone to low voltage than others. We measured the error rate of 10 different pages of flash memory across a voltage range of 1.6 V–2.2 V. While the conditions are kept consistent for all pages, one particular page had always about four times higher write error rate than the average of other pages. An error-aware storage design can avoid more error-prone pages at low voltages to increase reliability.

MLC flash memory stores more than one bit of information from one flash cell. For example, the flash memories we tested achieve two bits of information by storing four states in one cell: 0x11 (fully erase), 0x10 (partially erase), 0x01 (partially programmed), 0x00 (fully programmed). We tested all (not fully erased) data patterns to the same page of flash memory for 100 rounds while varying voltage. The average error rate for each

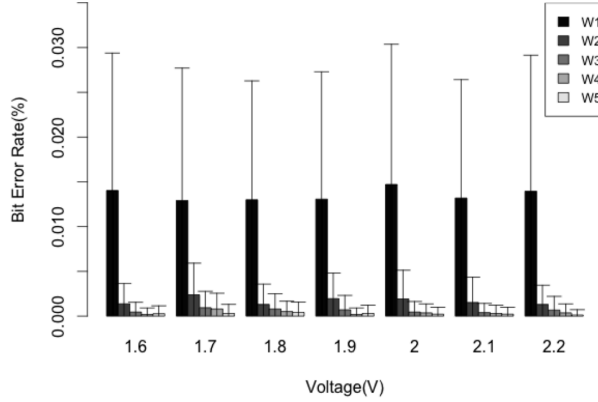


Figure 2: Reliability improvement using in-place writes over five different voltage for a MLC.

pattern is about the same for each voltage level, which means the pattern of the data being stored in flash memory does not affect the error rate noticeably.

Previous work [2] shows that NOR flash memory can be operated at low voltages but they are more sensitive to voltage than NAND flash memory. Work of Wei et al. [3] evaluates the behavior of NAND flash memory under fluctuating voltage and it shows that energy efficiency can be improved by operating at low voltages if the voltage is not changing too quickly. Our work examines the flash memory at fixed low voltages. Retention relaxation [1] increases the program step voltage to make the *write* faster at the cost of shorter retention time.

## Reliable Low-Voltage Storage With No HW Modification

The reliability of a low-voltage operated NAND flash memory can be further improved using a software-only method of in-place writes: rewriting data in the same memory location more than once to allow for more charge to be stored in flash cells. For example, by repeating the *write* only a second time, the error rate at 1.7 V goes to 0.002%. Figure 2 shows the effectiveness of repeating the writes to compensate for the errors.

## Evaluation of Energy Savings and Latency

We have measured the energy consumption and latency of one-page of flash writes using an oscilloscope and a sense resistor. We measured the voltage over the sense resistor and the time needed to finish writing to 10 pages. We then calculated power and energy as follows (and then got the average of 10 pages). We repeated the measurements for the voltage range of 1.6 V–2.8 V. Figure 3 shows that under-volting flash memory reduces the energy consumption by 40% if voltage is reduced from

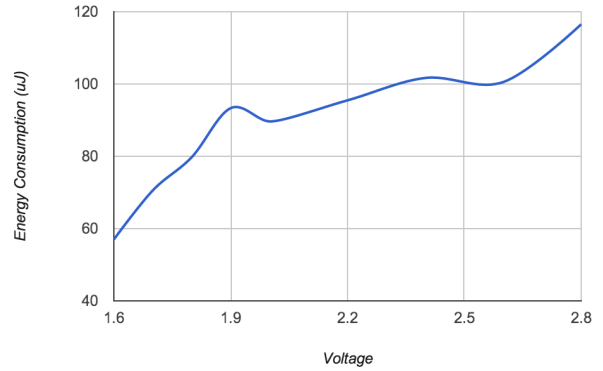


Figure 3: Energy consumption of writing a page (1024 bytes) at voltage range of 1.6 V–2.8 V.

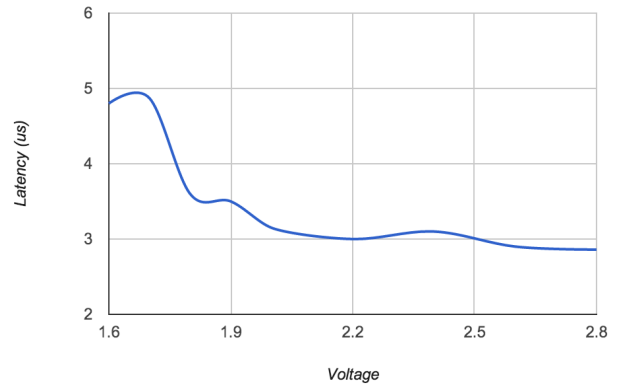


Figure 4: Latency of writing a page (1024 bytes) at voltage range of 1.6 V–2.8 V.

2.8 V to 1.7 V while the latency of flash writes (Figure 4 increases by 40%, and 45% improvement in power consumption. This make our proposed method most suitable for systems with power and energy as their priority. The increase in latency is partially because the hardware repeats the writes in case there are errors in flash writes.

## References

- [1] LIU, R. S., YANG, C. L., AND WU, W. Optimizing nand flash-based ssds via retention relaxation. In *Proceedings of the 10th USENIX Conference on File and Storage Technologies (FAST '12)*.
- [2] SALAJEGHEH, M., WANG, Y., FU, K., JIANG, A. A., AND LEARNED-MILLER, E. Exploiting half-wits: Smarter storage for low-power devices. In *Proceedings of the 9th USENIX Conference on File and Storage Technologies (FAST '11)* (San Jose, CA).
- [3] TSENG, H.-W., GRUPP, L. M., AND SWANSON, S. Underpowering nand flash: Profits and perils. In *DAC'13* (May 2013).

## Notes

<sup>1</sup>The author was a postdoctoral associate at UVA during this work.