Measuring Parameter Variation on an FPGA Using Ring Oscillators

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Abstract

As processor clock frequencies become faster, architecture-level design is becoming increasingly limited by factors such as on-chip variation. Parameter variation occurs in integrated circuits as the result of a variety of manufacturing and physical factors. In this paper, we examine the degree to which there is parameter variation on an FPGA. Data were gathered from a combinatorial logic device instantiated on the FPGA. We analyze these data with respect to variance, and provide a confidence interval for the variance and standard deviation.

1 Introduction

As microprocessor die sizes grow smaller, and clock speeds are made faster, designs are becoming increasingly limited by physical constraints. Since clock speeds must be set to accommodate the worst case, a critical path, any uncertainties introduced as a result of the nature of the material or the design process must be taken into account in the design process. This deviation from design parameters originates as a result of one of two causes: environmental factors or physical factors. Environmental factors consist of variations that occur as a result of the operation of the circuit, such as a variable voltage supplied by the power supply, or differences in ambient temperature. Physical factors refer to variations that are introduced as a result of deviations in the material due to materials and the method of manufacture.

Models describing the effects of variability on power and performance have been extensively studied at the microarchitecture level by Marculescu *et al.* [1]. Various techniques were explored, such as using different clocks to reduce temperature variability in hotter structures, and dynamic voltage scaling (DVS). Gate length variability, as well as thermal effects on clock speedup were taken into account when determining the maximum critical path and maximum clock speed. Benchmarks were run on a simulator to compare the different energy-aware design methodologies. The conclusion

detailed the improvements of each of the variability models over baseline in terms of a quality metric Q defined as:

$$Q = Energy * DieArea * T_{cp,max} * CPI \quad (1)$$

Where $T_{cp,max}$ * CPI is the critical path times cycles per instruction (representing performance), and energy, die size are weighted equally with it in the metric.

The effects of inter-die and intra-die variations on pipeline performance were investigated by Datta *et al.* [2]. When using pipelines to increase throughput, which has become a common practice in microprocessor design, the clock frequency is limited by the pipeline stage with the maximum combinatorial delay. Therefore, in high-performance design, it is necessary to determine the precise impact this variation will have on delay. Datta points out that physical factors such as variation in channel length/width, and thus threshold voltage, will lead to uncertainty in determining stage delay, which will adversely affect the pipeline delay, since the slowest stage may not be apparent. Datta takes parameter variation into account and presents an algorithm for maximizing yield. Aside from the trade-off between number of pipeline stages and logic depth that is fundamental to design of any pipelined processor, the paper also covers a trade-off between mean delay and the effect of variability. Normally, pipeline stages are designed in such a way that their delays are similar (balanced) and thus throughput can be maximized by setting a faster clock. This paper argues that by introducing an imbalance by increasing area in one stage and decreasing it in another can mitigate the effects of variation. The reason for this is that a balanced pipeline will tend to have more critical paths, and there will be more variation as a result.

A statistical description of parametric variation was presented by Boning in [3]. Separating variation into two groups, inter-die and intra-die, Boning *et al* examines the sources of variation that are present in integrated circuit devices. For example, deviations in the dopant used to fabricate a device have an impact on the threshold voltage, V_{th}. Due to the nature of the technology, small changes in dimensional properties such as channel width, as well as random fluctuations in electrical properties such as resistivity, leakage current, and dielectric constant can introduce variations that will affect the behavior of the device as a part of an integrated circuit. Boning favors worst-case analysis techniques due to the costs and low availability of parameter statistics that are accurate and current. The models described in the paper relate to random, correlated, and spatial variation.

2 Design

As discussed earlier, parameter variation related to electrical properties affects quantities like V_{th}, and therefore the operating characteristics of a device will vary as a result. Since this variation affects delays, it can be represented by finding the frequency at which a combinatorial structure will operate. A simple component exemplifying

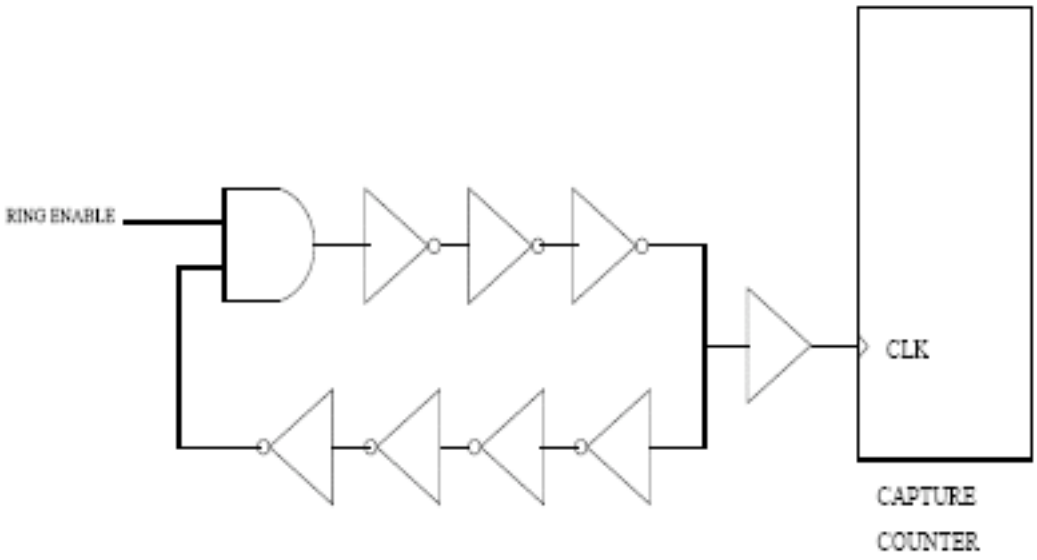

Figure 1: Diagram of ring oscillator (taken from [4])

combinatorial elements is a ring oscillator, in this case implemented as a string of inverters.

The ring oscillator sensors used in this project were adapted from an earlier design by Velusamy *et al* in [4]. Fundamentally consisting of inverters implemented in look up tables (LUTs), relative location (RLOC) parameters were used to equalize the on-chip distance between the inverters. This was done to ensure that the distances between the nodes on the sensor were as uniform as possible. In this design, the RLOC parameter was made into a parameter that can be passed to the device by the synthesis tool, in case the internal components need to be arranged to fit custom constraints where they would otherwise be "misplaced" by the design tool's place and route (PAR).

A Field-Programmable Gate Array (FPGA) provides an ideal platform for collecting sensor data for several reasons. The ring oscillator can be instantiated at any point on the chip, and runs on the same fabric as the processor and the rest of the peripherals. Because the device is programmed prior to gathering data, there are no fabrication costs associated with running such programs. The FPGA used in this project was an XUP Virtex II Pro.

To measure the variation due to physical factors, a ring oscillator was placed at different locations on the FPGA, and a diagnostic program run. A reading of the ring oscillator's freqency in terms of the system clock speed was taken from a certain time range that was found to have stable values [4]. Since the goal of this project

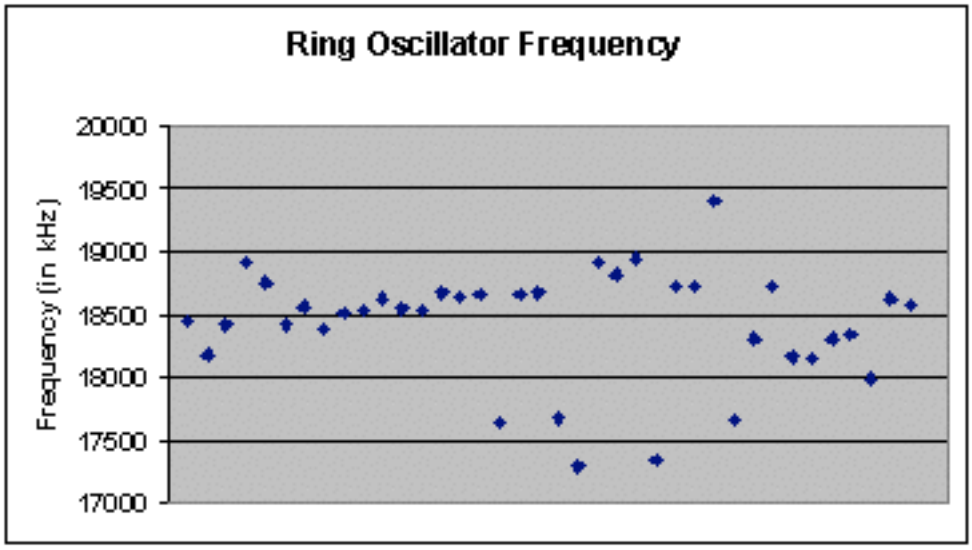

Figure 2: Ring Oscillator Frequency Sampled on the Virtex II FPGA

was to measure the variation due to physical factors, an effort was made to keep environmental factors constant from one sensor reading to the next. Use of ambient temperature control and power regulation beyond what was available on the board was not deemed necessary; for these measurements, only the differences in readings were important. That is, as long as no environmental variations were introduced between readings, data taken should be reasonably accurate.

3 Data

The data, measured in kHz, has a distribution as shown in Fig. 2:

Assuming the physical variations on the chip result in a normally distributed set of values for a small sample size, the t distribution should fit the data obtained. To determine the confidence interval for the variance σ^2, we use the chi-squared distribution:

$$(n-1)s^2/\chi^2_{\alpha/2,n-1} \text{ for the lower limit, and} \tag{2}$$

$$(n-1)s^2/\chi^2_{(1-\alpha/2),n-1} \text{ for the upper limit.} \tag{3}$$

The population has an experimental standard deviation s of 446.55, and 37 degrees of freedom. The 95% confidence interval for the variance σ^2 then has a lower and upper limit of 132537.1 and 333768.1 respectively. This yields a 95% CI for σ equal to (364.1,577.7).

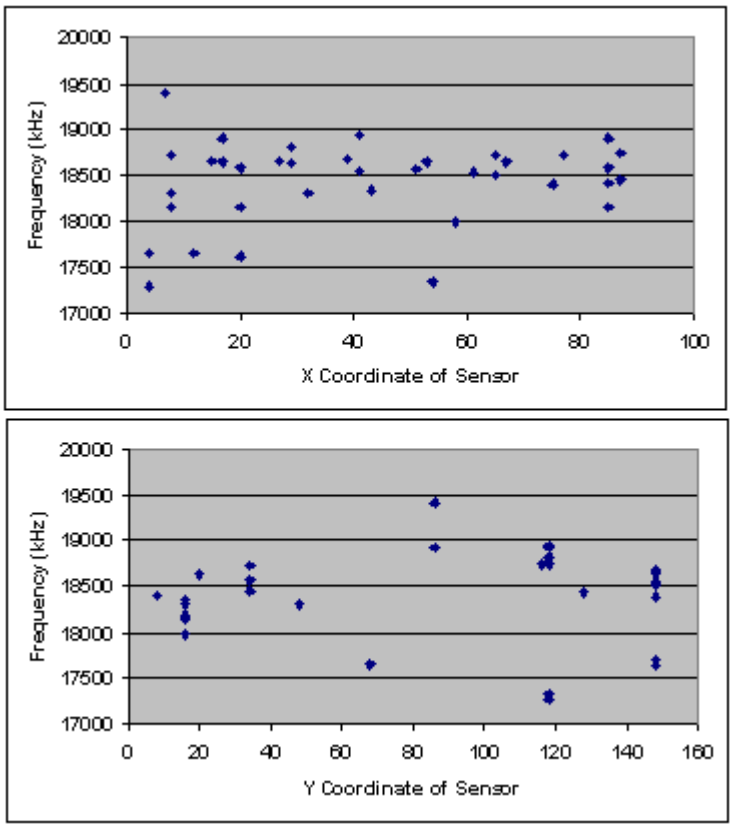

Figure 3: Ring Oscillator Frequency Versus Location on FPGA

It is also useful to plot ring oscillator frequency versus physical location on the chip. Excluding minor variations in the position of the sensor due to place-and-route restrictions on the FPGA, the ring oscillator's location can be described as an x,y coordinate pair referring to an absolute location on the device with the origin at the lower left of the device.

There are no obvious trends on the FPGA with respect to position. The incidence of high frequencies at locations with a y coordinate near 90 likely are the result of heating on the device; that area was densely populated with instantiations of blockRAM controllers, etc.

4 Conclusion

We used ring oscillators as sensors on an FPGA and took data on their operating frequency. As noted in [3], it is often difficult to obtain accurate data, and there are a variety of environmental factors such as temperature [4] that can have an impact on the performance of the ring oscillators. Taking into account the potential inaccuracy

in taking measurements on the board, we concluded that the variance due to physical factors is between the values shown above.

5 References

[1] D. Marculescu, E. Talpes. "Variability and Energy Awareness: A Microarchitecture-Level Perspective." In *Proc. Design Automation Conference (DAC)*, 2005

[2] A. Datta, S. Bhunia, S. Mukhopadhyay, N. Banerjee, and K. Roy. "Statistical Modeling of Pipeline Delay and Design of Pipeline under Process Variation to Enhance yield in sub-100nm Technologies." In *Proc. Design and Test in Europe (DATE)*, 2005

[3] D. Boning and S. Nassif, "Models of Process Variations in Device and Interconnect," Ch. 6 of Chandra, *Design of High-Performance Microprocessor Circuits.*

[4] S. Velusamy, W. Huang, J. Lach, K. Skadron, "Monitoring Temperature in FPGA Based SoCs," CS Technical Report CS-2004-39, 2004.

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