EXPERIENCES USING FPGAS FOR TEMPERATURE-AWARE MICROARCHITECTURE RESEARCH

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Ever increasing microprocessor power densities has brought temperature-aware microarchitecture research to the forefront. In this paper, we describe our experiences in creating an FPGA based testbed suitable for studying on chip thermal phenomena. The testbed features the ability to implement small and accurate temperature sensors at any location on the die. Implementing such sensors along with soft-processors provides a vehicle to perform temperature aware micro-architecture research. We illustrate the utility of such a setup by using it to perform dynamic thermal management (DTM).

Decreasing feature sizes coupled with higher clock rates has resulted in exponentially increasing power densities in current generation microprocessors. The high power density manifests itself as heat which has to be constantly removed via sophisticated packaging techniques to maintain the health of the processor. Many microarchitectural techniques have been proposed [1, 2] that attempt to tackle this problem. To facilitate research in temperature-aware computing, we developed a thermal model - *HotSpot*, that can be integrated with microarchitectural simulators [3]. While *HotSpot* has been validated against a test chip [4], our original motivation for this work was to validate *HotSpot* with more realistic processors. Although current generation microprocessors include some form of temperature sensing capability, they are not useful for identifying temperature gradients since very few on-die sensors are present.

The testbed consists of a parametrizable number of temperature sensors that are implemented on the FPGA. Each temperature sensor is a ring oscillator whose output frequency is directly proportional to the operating temperature [5]. While implementing such oscillators, attention has to be given to maintain consistent routing paths between various instances of the sensors. The sensors are then calibrated by placing the test setup in a temperature controlled oven and noting the frequency response with temperature. In our experiments, we noticed a change of 380 KHz corresponding to a degree change in temperature. The sensor has enough resolution to show changes of less than 0.1 C. The temperature sensors have a simple interface through which a microcontroller or a microprocessor can obtain the current die temperature, and take appropriate action.

We have found such a setup to be very useful for research purposes. For example, experimentally we can show that hotspots that are smaller than 32 slices in area (in a Xilinx XC2VP7 device, approximately equal to 1% of the device) do not increase the temperature of the die, if they are sorrounded by cooler units. The implication for computer architects is that small units which have a high power density, like the register file, can be subdivided into smaller units and interspersed with other cooler units.

The FPGA device used in our experiments has support to implement DTM techniques like clock gating and coarse grained frequency scaling. These techniques can be controlled by a processor, hence providing an easy way of experimenting with different control strategies. While our experience using FPGAs for thermal research has been mostly positive, there are two main obstacles we need to resolve for this solution to be more useful: First, the power density levels on the FPGA are lower when compared to a custom circuit. This is because of the area inefficiency of FPGAs. Second, complex microprocessor models are not available in a form that can be synthesized to FPGAs. This limits the parameter space that architects can experiment with.

To summarize, we have come up with the design of an FPGA testbed that is suited for use in temperature-aware computing research. We have shown that such a testbed can be used for:

- Showing that small hotspots can be mitigated by sorrounding them with cooler units.
- Experimenting with different DTM control techniques.
- Validating thermal models. In our experiments we have found *HotSpot* to predict temperatures within 10% of the temperatures obtained by the sensors.

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