CS3330 Exam 2 – Spring 2015

Name: _____

Directions: Put the letter of your selection or the short answer requested in the box. **Write clearly**: if we are unsure what you wrote you will get a zero on that problem.

There are several variants of this exam being given at the same time. Copying from your neighbor is not only cheating, it is also foolish.

Test proctors will *not* provide clarification during the exam. If you find something **ambiguous** or unclear, explain that clearly on your exam and add a * to the top right corner of your answer box so we know to look for your note when grading.

Unless otherwise specified, all questions assume a **little-endian** computer.

If you do not sign the pledge on the last page you will get a zero on the entire exam.

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Question 1: Your code intentionally keeps addresses far from one another to foil certain kinds of security vulnerabilities. Your data accesses can benefit from

A temporal locality
B spatial locality
C both of the above
D none of the above

Answer:

Question 2: Suppose the decode phase takes a variable number of cycles. If it signals that it needs another cycle to finish its work, which pipeline registers should be bubbled?

A all of those after decode
B just the one right after decode
C all those before decode
D just the one right before decode

Answer:

Question 3: Your code never accesses the same address twice; it can benefit from

A spatial locality
B temporal locality
C both of the above
D none of the above

Answer:

Question 4: Suppose in 2000 you wrote some that code reads a value from memory, does some computations, then reads another value, etc. At that time your code spent 50

A Spend most of its time computing
B Spend most of its time accessing memory
C Still be well balanced between memory access and processing

Answer:

Question 5: When given neither bubble nor stall inputs, a pipeline register outputs

A the same thing it outputted last cycle
B nop
C its input

Answer:

Question 6: What is the difference between a data dependency and a data hazard?

A a hazard is a property of a pipeline, a dependency is a property of code
B no difference, they mean the same thing
C a hazard is a property of a code, a dependency is a property of pipeline
D a dependency requires special handling; it is only a hazard if it doesn't get handled correctly

Answer:

Question 7: Your code multiplies each element of a large array by 2. Your array accesses can benefit from

A spatial locality
B temporal locality
C both of the above
D none of the above

Answer:

Question 8: The CPU is attached to which of the following busses? Select all that apply.

A System bus
B School bus
C CPU bus
D I/O bus
E Memory bus

Answer:

Question 9: Which of the following are reasons to have separate instruction and data caches?

A access patterns are different so different cache organisations (set size, etc) make sense
B you don't want your data and cache accesses to conflict with one another
C you don't usually access code as data so you won't get many extra hits if you merged them
D they are on separate memory chips so they have to have separate caches
E each core should have its own instruction cache but they all share one data cache

Answer:

Question 10: Organize the following kinds of storage from fastest to slowest. Do this by writing four letters in order in the box.

A SRAM
B Magnetic disk
C DRAM
D Solid-state disk

Answer:

Question 11:

When a dependency has the potential to cause incorrect computation in a pipeline, it is called a _____ (write your answer in the box).

Answer:

Question 12:

A write-_____ cache immediately forwards writes to the next larger cache. (write your answer in the box)

Answer:

Question 13: A pipeline register is currently emitting an `addl` instruction and is being given a stall signal with an `xorl` instruction as its input. What code does it emit next cycle?

A `addl`
B `bubble`
C `xorl`
D `stall`
E `nop`
F None of the above

Answer:

Question 14: Suppose address *A* and *B* differ only in the tag part of the address. Which of the following read sequences has exactly one conflict miss?

A Read *A*, then read *B*, then read *A*, then read *B*
B Read *A*, then read *B*
C Read *A*
D Read *A*, then read *B*, then read *A*

Answer:

Question 15: Consider choosing between two caches with the same capacity and access time: one fully-associative and one direct-mapped. If your code never accesses the same address twice, which will result in fewer cache misses?

A direct-mapped caches
B fully-associative
C they are the same
D insufficient information to tell

Answer:

Question 16: When given a bubble signal, a pipeline register outputs

A its input
B the same thing it outputted last cycle
C nop

Answer:

Question 17: A fully-associative cache is like a

A set-associative cache with only one line per set
B direct-mapped cache with only one set
C set-associative cache with only one set
D direct-mapped cache with only one line per set

Answer:

Question 18: Suppose we have an ALU that might take several cycles to process a single operation. The ALU has an output signal `busy` that is 1 if it needs another cycle with the same operation, 0 if it is ready for a new operation next cycle.

Consider a pipeline register several stages after the execute phase. What best describes how that register should react to a 1 in the `busy` bit?

A stall
B bubble
C normal operation
D it depends on if this is the first busy for this operation or not

Answer:

Question 19: Suppose your program accesses a large set of bytes of memory; each byte is far from others accessed but each is accessed many times. Assuming you cannot change the size of your cache, which of the following characteristics of the cache will help the program run faster?

A large blocks
B small blocks

Answer:

Question 20: Suppose we have an ALU that might take several cycles to process a single operation. The ALU has an output signal `busy` that is 1 if it needs another cycle with the same operation, 0 if it is ready for a new operation next cycle.

Consider the pipeline register at the end of the execute phase. What best describes how that register should react to a 1 in the `busy` bit?

A stall
B bubble
C normal operation
D it depends on if this is the first `busy` signal emitted by the ALU for this operation or not

Answer:

Question 21: Suppose addresses A and B both map to the same line of a direct-mapped cache but with different tags. Code reads A once then reads B once. The read of B is a

A conflict miss
B cold miss
C hit
D capacity miss

Answer:

Question 22: Select all of the following that are true.

A A set-associative cache with one set is a direct-mapped cache
B A set-associative cache with one set is a fully-associative cache
C A set-associative cache with one line per set is a fully-associative cache
D A set-associative cache with one line per set is a direct-mapped cache

Answer:

Question 23: Suppose we have an ALU that might take several cycles to process a single operation. The ALU has an output signal `busy` that is 1 if it needs another cycle with the same operation, 0 if it is ready for a new operation next cycle.

Consider a pipeline register earlier in the pipeline than the ALU. What best describes how that register should react to a 1 in the `busy` bit?

A it depends on if this is the first `busy` signal emitted by the ALU for this operation or not
B stall
C bubble
D normal operation

Answer:

Question 24: Organize the following kinds of storage from cheapest to most expensive by byte. Do this by writing four letters in order in the box

A SRAM
B Magnetic disk
C Solid-state disk
D DRAM

Answer:

Question 25: When given a stall signal, a pipeline register outputs

A nop
B the same thing it outputted last cycle
C its input

Answer:

Question 26: Select the most correct statement from the following as applied over the last two decades:

A Processors get faster but memory does not
B Processors and memory both get faster, but processors get faster faster than memory does
C Memory gets faster but processors do not
D Processors and memory both get faster, but memory gets faster faster than processors do

Answer:

Question 27: Suppose addresses A and B both map to the same line of a set-associative cache but with different tags. Code reads A, then B, then A, then B. The second read of B is a

A conflict miss
B cold miss
C capacity miss
D hit

Answer:

Question 28:

A 10-bit address is sent to a cache with 8 sets of 2 lines; each block has 8 bytes. How many bits long is the tag?

Answer:

Question 29:

A 12-bit address $ABCDEFGHIJKL$ (where each letter represents a single bit) is sent to a cache with 2 sets of 8 lines each; each block has 4 bytes. What is the set index? (if you think it is the first three bits, you would answer ABC)

Answer:

Question 30: How would a program decide if it queries the instruction cache or the data cache?

A it tries both and sees which one has a hit
B there's not a best choice; each chip designer picks one based on their use case.
C it decides based on the pipeline stage that issues the request
D it decides based on the address used

Answer:

Question 31: Pipelining generally

A reduces throughput and reduces latency
B reduces throughput and increases latency
C increases throughput and increases latency
D increases throughput and reduces latency

Answer:

Question 32:

A 12-bit address is sent to a cache with 4 sets with 16 lines per set; each block stores 32 bytes. How many bits long is the tag?

Answer:

Question 33: Consider a two-stage pipeline: one stage has fetch and decode, the other has execute, memory, and writeback. Condition code information is available at the end of the execute phase and might be needed at the beginning of the fetch stage of the next instruction. Using data forwarding, the pipeline-introduced delay associated with a branch would be at most

A 2 cycles
B 1 cycle
C 0 cycles

Answer:

Question 34: Consider a longer pipeline: F, D, E, Mr, Mw, W, where memory read and memory write have been split into two phases to facilitate memory-memory moves. Data needed in the E phase is always from a register, and new register values can can appear in the D, E, or Mr phases. If we have data forwarding, what is the largest data dependency delay we could see?

A 5 cycles
B 3 cycles
C 1 cycle
D 4 cycles
E 2 cycles
F no delay
G 6 or more cycles

Answer:

Question 35: Imagine a 10-stage pipeline where an instruction could depend in the beginning of stage 5 on the results of the previous instruction in then of stage 8. If we have data forwarding, how many cycles does this dependency waste?

A 9 or more
B 0 or 1
C 4
D 2
E 3
F 5
G 6, 7, or 8

Answer:

Question 36: A pipeline register is currently emitting an `addl` instruction and is being given neither a bubble nor a stall signal, with an `xorl` instruction as its input. What code does it emit next cycle?

A `nop`
B `stall`
C `bubble`
D `addl`
E `xorl`
F None of the above

Answer:

Question 37:

A 12-bit address *ABCDEFGHIJKL* (where each letter represents a single bit) is sent to a cache with 16 sets of 1 line each; each block has 32 bytes. What is the block offset? (if you think it is the first three bits, you would answer *ABC*)

Answer:

Question 38: The I/O Bus connects the disk, USB, network card, and graphics card to which other computer component?

A I/O Bridge
B CPU
C Main Memory
D Bus Interface
E Schoolhouse

Answer:

Question 39: A pipeline register is currently emitting an `addl` instruction and is being given a bubble signal with an `xorl` instruction as its input. What will it emit next cycle?

A `addl`
B `stall`
C `xorl`
D `bubble`
E `nop`
F None of the above

Answer:

Question 40: Consider a longer pipeline: F, D, E, A, M, W, where the A phase does some kind of address computation. Data needed in the E phase is always from a register, and new register values can can appear in the D, E, or M phases. If we do *not* have data forwarding (i.e., we stall any time data we need is not where we need it), what is the largest data dependency delay we could see?

A 0 cycles
B 6 cycles
C 3 cycles
D 4 cycles
E 2 cycles
F 1 cycle
G 5 cycles

Answer:

Question 41: Starting from a cold cache, your program accesses one byte at a time in order from address 0x000 to address 0x100, then terminates. Which of the following characteristics of the cache will help the program run faster? (pick all that apply)

A large blocks
B more lines per set
C small blocks
D more sets
E none of the above will help

Answer:

Question 42: Suppose the memory phase takes a variable number of cycles. If it signals that it needs another cycle to finish its work, what should we do with the pipeline registers before it?

A bubble
B stall
C different pipeline registers should get different signals
D normal operation

Answer:

Pledge:

On my honor as a student, I have neither given nor received aid on this exam.

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