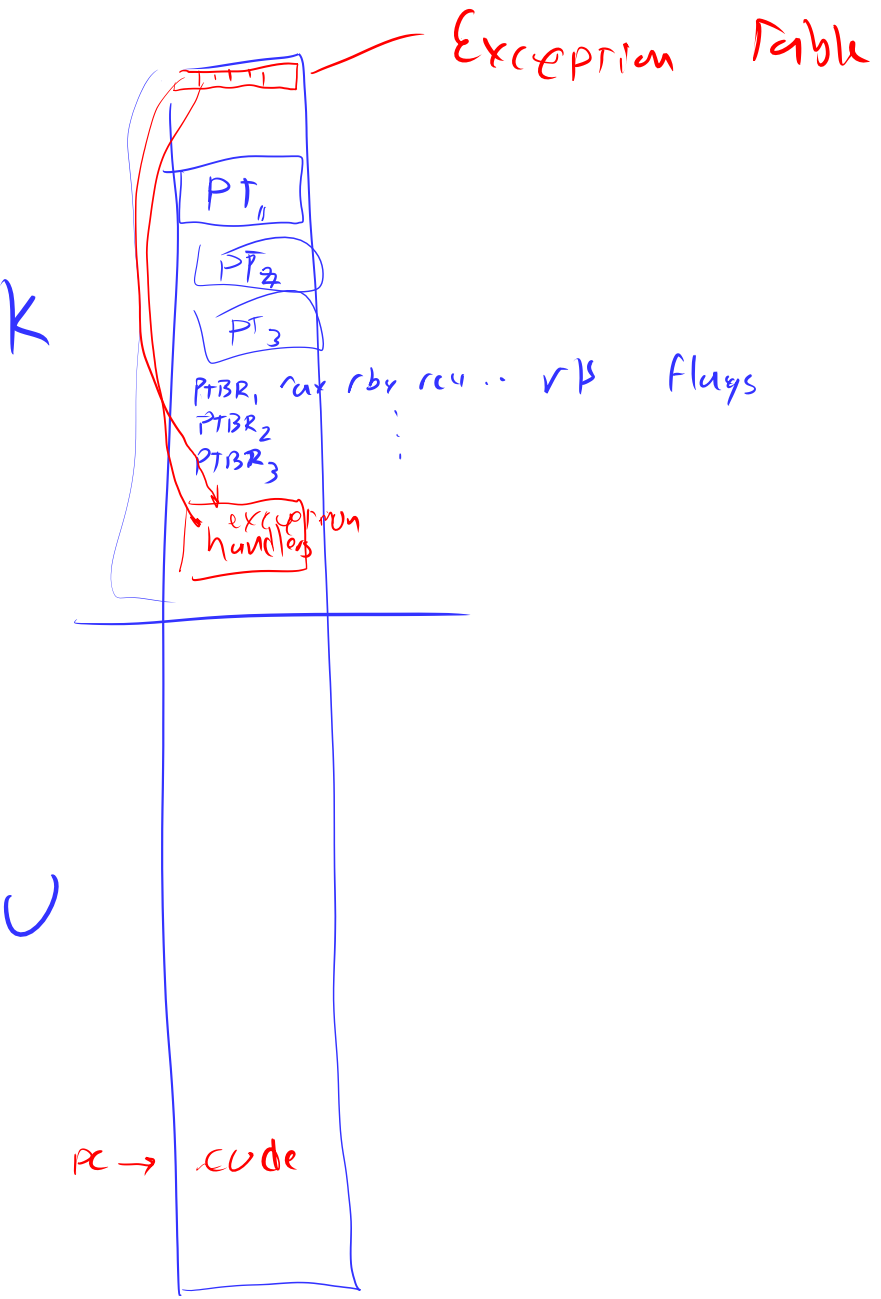
Exceptions:

1. faults — fix & re-run
   - Caused by instruction that sometimes succeeds
   - ÷0
   - Page fault
2. interrupts — invisible → or about usually
   - Caused outside the code
   - timer
   - keys
   - continue
3. traps — looks like call
   - Caused by an instruction that always fails
   - Syscall
   - continue with changed state

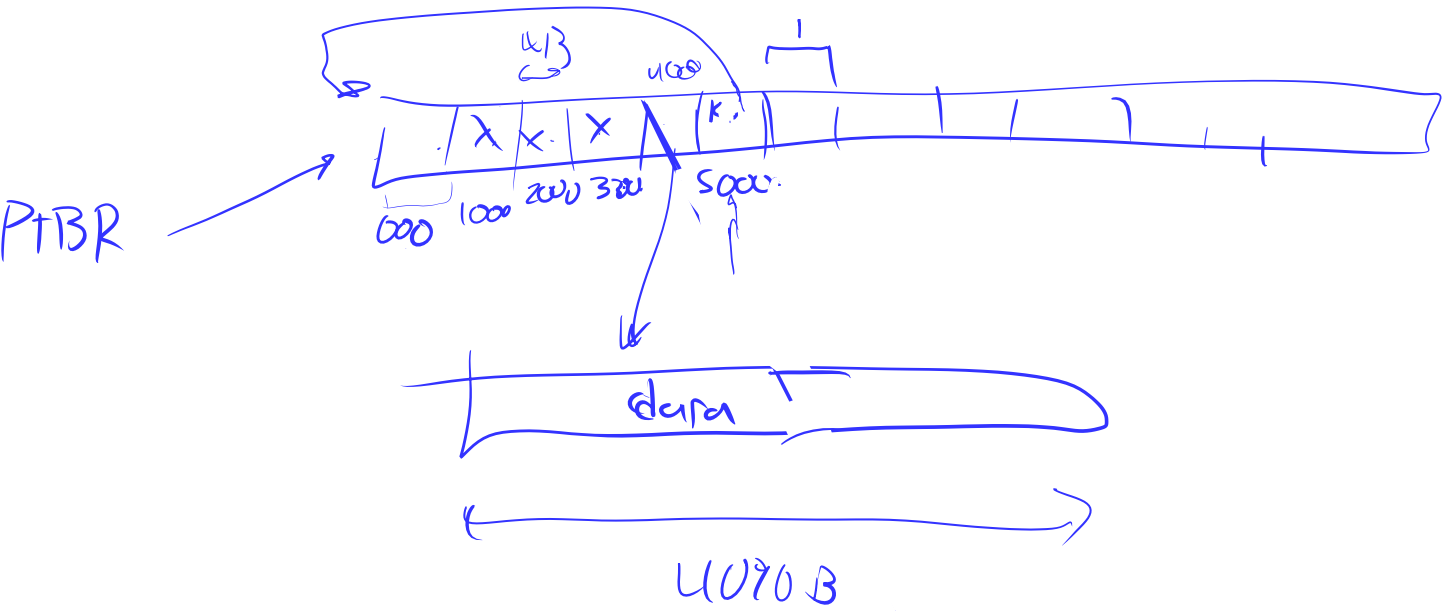


HW on exception

1. Suspend your code
   - Copy of PC, reg, Flags
2. look up handler in exception table
3. in kernel mode, call handler

Single-level PT

mov %rdi, 0x5014



L1, L2...

TLB vs other cache

TLB has no block

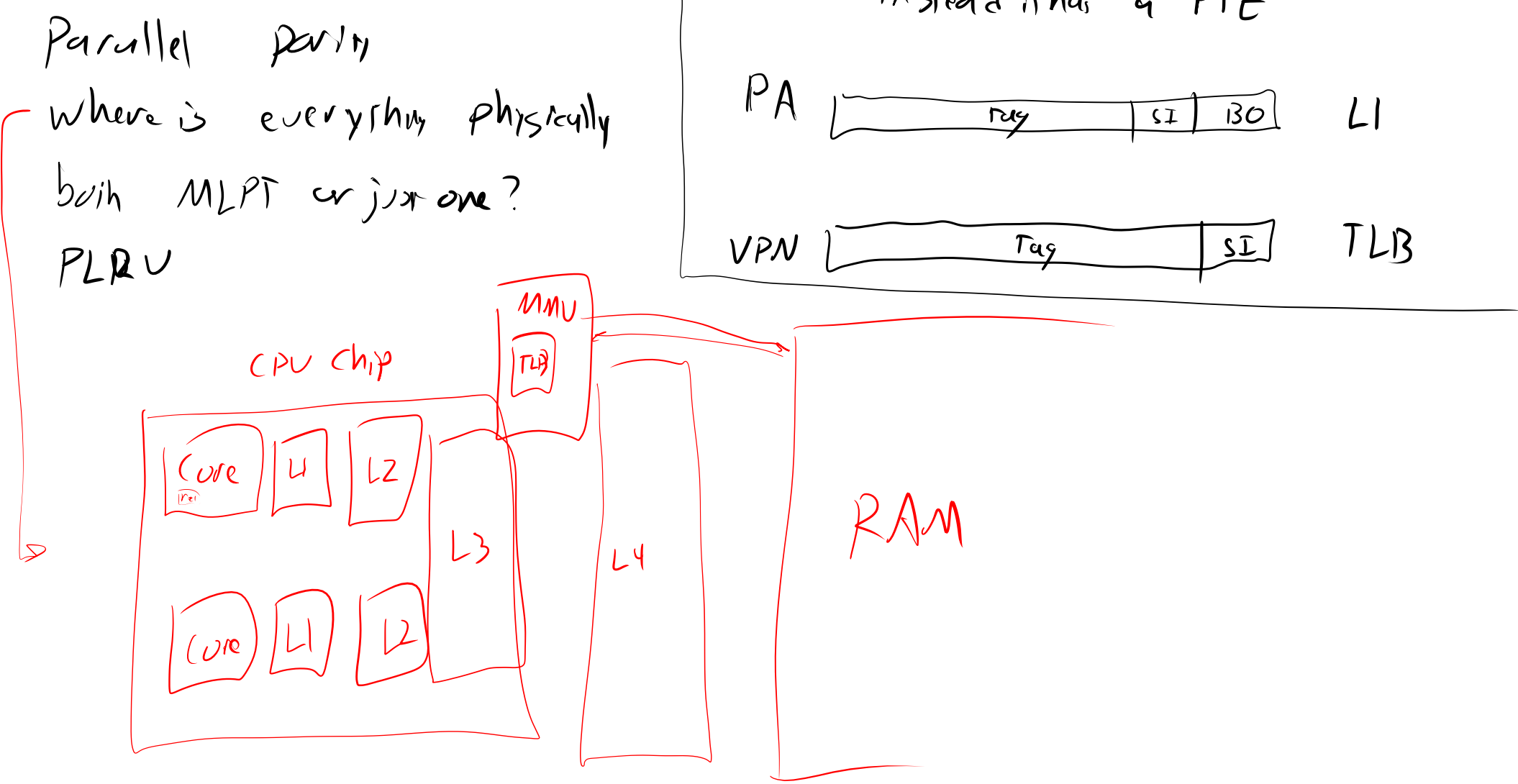
instead it has a PTE

Parallel path

where is everything physically

both MLPT or just one?

PLRU



Parity $(x >> 16) \wedge x$