

## BRUCE R. CHILDERS

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### OBJECTIVE

*Tenure-track assistant professor* with a speciality in compilers/computer architecture.

### PROFESSIONAL INTERESTS

Compilers and software development tools, computer architecture, application-specific and reconfigurable processors, electronic design automation, processor and system simulation, and embedded and portable computer systems.

### EDUCATION

Ph.D. (Sept. 1991–present), Computer Science, **University of Virginia**, Charlottesville, Virginia. Thesis title: “Custom pipelines for embedded applications.” Advisor: Prof. Jack W. Davidson. Expected Spring 1999.

B.S. (May 1991), Computer Science, **College of William and Mary**, Williamsburg, Virginia. Graduated *cum laude*. Honors advisor: Prof. Phil Kearns.

### RESEARCH EXPERIENCE

*Research assistant* (May 1992–present), University of Virginia, Computer Science Department; Supervisor: Prof. Jack W. Davidson.

- Researching architectural synthesis of custom instruction-level parallel processors for embedded systems.
- Developed a new computer microarchitecture called “wide counterflow pipelines” for synthesis of very long instruction word (VLIW) embedded processors.
- Developed a novel hardware/software co-design system (implemented in Java, C++) for automatically deriving application-specific integrated processors using design space exploration and software pipelining.
- Developed a new simulation technique based on resource tiling for very fast and reconfigurable behavioral simulation of counterflow pipelines.
- Developed an object-oriented execution-driven counterflow pipeline simulator (implemented in C++).
- Developed web-hosted performance analysis, trace viewing, and archival tools for processor design.
- Retargeted *lcc/vpo* C compiler to Motorola 68HC05 MCU.

**RESEARCH EXPERIENCE (CONTINUED)**

*Research intern* (May–Oct. 1996, June–Aug. 1997), Hewlett-Packard Laboratories, Compiler and Architecture Research, Palo Alto, California; Manager: Dr. Bob Rau.

- Participated as member of research group developing a system for automatic synthesis of high-performance application-specific processors (VLIW/systolic array architecture).
- Developed and implemented compiler loop transformations (using the SUIF compiler) for reducing the number of structural elements in a synthesized systolic array processor.
- Developed and implemented a structural intermediate representation for compiler-based systolic processor synthesis.
- Developed translator for generating VHDL from a processor description; implemented VHDL models of processor functional units; integrated end-to-end processor synthesis system.

*MIS programmer* (Summers 1993–1995), Motorola, Inc., Corporate Software Research and Development, Software Systems Research Laboratory, Schaumburg, Illinois; Manager: Dr. John Barr.

- Researched and implemented machine dependent compiler optimizations in *gcc* for a low-power embedded communications processor.
- Retargeted the GNU *gcc* compiler to a new embedded RISC microprocessor; delivered compiler to internal Motorola customers.
- Supported instruction set experimentation with *gcc*; retargeted GNU *gld* linker and *gas* assembler to the ARM 610 processor; assisted in porting of SPEC benchmark suite and C library to a new processor.
- Verified functional and timing correctness of an embedded system simulation environment; developed behavioral simulation models of the Motorola Bravo Express pager and Motorola HC05 microprocessor.

**TEACHING EXPERIENCE**

*Teaching assistant* (Spring 1996), CS216 Computer Data Representation, University of Virginia, Instructor Prof. Wm. A. Wulf.

- Supervised four undergraduate teaching assistants, supervised and lead two weekly programming laboratories (lecture/hands-on, 30 students), assisted students, graded coursework.

*Teaching assistant* (Fall 1996, Spring 1994), CS101 Introduction to Computer Programming, University of Virginia, Instructor Prof. Jack W. Davidson.

- Developed and implemented programming and course projects (10 assignments, 100 students in 3 class sections), graded coursework.

*Teaching assistant* (Spring 1992), CS210 Introduction to Computer Science, University of Virginia, Instructor Prof. Tom Olson.

- Held weekly office hours, conducted exam recitations (30 students), graded coursework, advised students.

**TEACHING EXPERIENCE (CONTINUED)**

*Technical consultant on a best-selling C++ college textbook* (Fall 1995), Charlottesville, Virginia.

- Developed a simplified MS Windows API and example applications for the introductory college textbook “C++ Program Design”, Jack W. Davidson and James P. Cohoon, McGraw-Hill.

*Senior thesis advisor* (Fall 1995, Spring 1996), advised undergraduate student on senior thesis, “Analysis of execution traces for counterflow pipelines”, faculty advisor Prof. Wm. A. Wulf, University of Virginia, Computer Science Department.

**OTHER PROFESSIONAL EXPERIENCE**

*Computer consultant* (Aug. 1989–May 1991), College of William and Mary.

*Retail software sales* (Feb. 1988–Aug. 1989), Egghead Discount Software, Falls Church, Virginia.

*Computer consultant* (Mar. 1986–Aug. 1989), Fairfax, Virginia.

*Computer technician* (June 1985–April 1986), Generation 5, Inc., Silver Spring, Maryland.

*Computer programmer* (Mar. 1984–Feb. 1985), Internal Revenue Service, Washington, D.C.

**PUBLICATIONS**

B. Childers and J. Davidson, “Automatic Design of Custom Wide-Issue Counterflow Pipelines”, submitted for publication, January 1999. Available from: <http://www.cs.virginia.edu/~brc2m/cfp>.

B. Childers and J. Davidson, “Architectural Considerations for Application-Specific Counterflow Pipelines”, to appear in *IEEE Conf. on Adv. Research in VLSI (ARVLSI'99)*, Atlanta, Georgia, March 1999.

B. Childers and J. Davidson, “A Design Environment for Counterflow Pipeline Synthesis”, *ACM SIGPLAN Workshop on Languages, Compilers, and Tools for Embedded Systems (LCTES'98)*, pp. 223–234, during *ACM PLDI-98*, Montreal, Canada, June 19–20, 1998.

B. Childers, J. Davidson, and W. Wulf, “Synthesis of Application-Specific Counterflow Pipelines”, *Workshop on Interaction between Compilers and Computer Architecture (INTERACT)*, during *IEEE HPCA-2*, San Jose, CA, February 4–8, 1996.

M. Alexander, M. Bailey, B. Childers, J. Davidson, and S. Jinturkar, “Memory Bandwidth Optimization for Wide-Bus Machines”, *Proc. of the 26th Annual Hawaii Int'l Conf. on System Sciences*, 1(1): 466–475, Wailea, Hawaii, January 1993.

B. Childers and J. Davidson, “Performance Evaluation of Wide-Issue Counterflow Pipelines”, in preparation for conference submission, January 1999.

## TECHNICAL REPORTS

B. Childers and J. Davidson, “Rapid Prototyping of Counterflow Pipelines”, UVA Computer Science Technical Report CS–99–01, January 1999.

B. Childers and J. Davidson, “Architectural Considerations for Application-Specific Counterflow Pipelines”, UVA Computer Science Technical Report CS–98–31, September 1998.

B. Childers and J. Davidson, “Application-Specific Pipelines for Exploiting Instruction-Level Parallelism”, UVA Computer Science Technical Report CS–98–14, May 1998.

B. Childers and J. Davidson, “A Design Environment for Counterflow Pipeline Synthesis”, UVA Computer Science Technical Report CS–98–05, March 1998.

B. Childers and J. Davidson, “Automatic Counterflow Pipeline Synthesis”, UVA Computer Science Technical Report CS–98–01, January 1998.

## TEACHING COMPETENCIES

### Undergraduate courses

- Introductory Computer Science (C, C++, Java)
- Computer Data Representation
- Computer Organization
- Computer Architecture
- Compilers
- Systems Programming/Software Development

### Graduate courses

- Computer Architecture (core and advanced seminars)
- Compilers (core and advanced seminars)

## SOFTWARE SYSTEMS

*wcfpsim* (Java, 17K lines), an extensible and highly reconfigurable simulator (using pipeline descriptions) for wide counterflow pipelines (includes graphical user interface and performance analysis components).

*wcfpsyn* (Java, 9K lines), a hardware/software co-design system for generating custom wide counterflow pipelines from an application’s source code using software pipelining and design space exploration.

*systolic synthesis* (C++, 5K lines), high-level loop code transformations implemented using the SUIF compiler for reducing amount of hardware generated for a custom systolic processor; Hewlett-Packard Laboratories, Palo Alto, California.

*AIR and VHDL generation* (C++, 5K lines), an architectural intermediate representation for systolic processor synthesis and an associated VHDL code generator; Hewlett-Packard Laboratories, Palo Alto, California.

## SOFTWARE SYSTEMS (CONTINUED)

*tview* (C++ and perl, 4.5K lines), a processor trace analysis and graphical viewing tool (emits HTML marked-up version of synthesis design space and processor execution traces and collects performance statistics).

*gcc*, a complete port of the GNU *gcc* C compiler to an embedded RISC communications engine; Motorola, Schaumburg, Illinois.

*cfpsim* (C++, 23K lines), a processor microarchitecture cycle-accurate simulator for counterflow pipelines.

*TargetBuilder*, an embedded system simulation environment; developed simulation models for a HC08 microcontroller and a Bravo Express pager; Motorola, Schaumburg, Illinois.

## PRESENTATIONS AND SERVICE

*Invited colloquium*, “Custom Counterflow Pipelines”, Hewlett-Packard Inc., Performance Delivery Laboratory, Cupertino, California, March 1998.

*Invited colloquium*, “Application-Specific Counterflow Pipelines”, Center for Computing Science, Institute for Defense Analysis, Bowie, Maryland, February 5, 1998.

*Invited colloquium*, “Counterflow Pipeline Synthesis”, Hewlett-Packard Inc., California Language Laboratory, Cupertino, California, August 1996.

*Guest lecturer*, Computer Organization (CS654), conducted class lecture on the UltraSPARC microprocessor, University of Virginia, Computer Science Department, Fall 1995.

*Poster presentation*, B. Childers, J. Davidson, and W. Wulf, “A Study on the Potential of Counterflow Pipelines for Application-Specific Microprocessors”, School of Engineering and Applied Sciences, presentation to IBM, University of Virginia, October 1995.

*Guest lecturer*, “Introduction to Makefiles”, presentation to new CS students (CS661), University of Virginia, Computer Science Department, October 1993.

*Honors defense*, “Source Code Compaction”, Department of Computer Science, College of William and Mary, Williamsburg, Virginia, April 1991.

## HONORS

B. Childers, “Source Code Compaction”, Honors thesis, accepted for Honors, College of William and Mary, Department of Computer Science, May 1991.

Award of Excellence, Internal Revenue Service, Washington, D.C., December 1984.

## ASSOCIATIONS

Member, Association for Computing Machinery (ACM)

Member, ACM Special Interest Group on Computer Architecture (SIGARCH)