

1. Consider a pipeline that has five stages: (1) instruction fetch – 30 ns, (2) instruction decode – 10 ns, (3) memory read – 30 ns, (4) instruction execution – 10 ns, and (5) register write – 30 ns. The times required in each stage are shown above following the name of the stage. For example, the instruction fetch requires 30 ns to complete. Assume that every instruction in the instruction set requires the use of all stages of the pipeline. Also, assume that the stages of the pipeline are clocked with a common clock. This means that all information moves synchronously through the pipeline from one stage to the next based on a single clock signal dictating when information advances from one stage to the next.

a. What is the latency of an instruction flowing through the pipeline? Again, remember that you have a common clock.

Answer: 30 ns * 5 stages = 150 ns

$1000 * (40 + 40 + 30) = 1000 * 110 = 110,000 \text{ ns}$

b. What is the idealized throughput (bandwidth) of the pipeline? (In other words, you may assume that there are no hazards between instructions for calculating this answer) 1000 insts

Answer: 1 instruction per cycle
 $1000 * 150 = 150,000 / 5 = 30,000 \text{ ns}$

~~110,000 ns~~
~~5 stages~~ ~~22,000 ns~~

c. What is execution time of 1000 inst program w/out pipelining?

d. Since all stages of the pipeline are clocked with a single clock signal, what is the fastest frequency of that clock for this pipeline?

Answer: 1 cycle / 30 ns

d. Assume that the following sequence of instructions is executed by the processor (assuming no hazards):

I1, I2, I3, I4

Using the table below, show the instruction that resides in each stage of the pipeline for each clock period.

why ^{IF} not ^{mem} exe _{MEM} WB ?

Clock Period	Instruction Fetch	Instruction Decode	Memory Read	Instruction Execution	Memory-Write Back
T1	I1				
T2	I2	I1			
T3	I3	I2	I1		
T4	I4	I3	I2	I1	
T5	I5	I4	I3	I2	I1
T6		I5	I4	I3	I2
T7			I5	I4	I3
T8				I5	I4

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