More on Caches  
Virtual Memory (cont’d)

Topics
• TDay Holiday Reading Assignment  
  – Read sections 6.1 and 6.4 in the textbook  
    • Number systems and radix conversion (6.1)  
    • Floating point representation and arithmetic (6.4)  
  – Potential final exam questions:  
    • Problems 6.1-6.3, 6.29, 6.30
• Caches wrapup  
  – Address generation  
  – A few more cache examples  
• Virtual Memory review  
  – Speeding up address translation

Last Friday - Class Participation 3
• 7.21  
  – 128 MB main memory  
  – 2 MB cache  
  – Blocks are 32 bytes in size  
  – byte addressable  
  Show the number of bits for tag, index, offset for:  
  – fully associative  
  – direct-mapped  
  – 8-way set associative

Address Generation (Direct-mapped)

Address Generation (8-way Set Associative)

Virtual Memory
Virtual Memory

Choosing Page Sizes

- Smaller page size
  - May increase number of page faults
    - More memory traffic
    - Increases size of page table (takes up more memory space)
- One solution: multilevel page tables
  - Highest level page table entry contains pointers to other page tables (tree)

Speeding up Address Translation

- Translation for each memory reference
- Each memory reference requires:
  - Page table access
    - to get page table entry
  - Access the memory location given the physical address calculated

  2 memory accesses == very slow
  Can this be sped up?

Question

- Memory is much cheaper now than in 1960s, do we still need virtual memory?

Translation Lookaside Buffer (TLB)

- Small “cache” (hardware)
  - stores most recent page table references
  - generally fully-associative
- TLB entry
  - contains virtual to physical page number translation

| Virtual Page number | A, P, D, U, V bits | Physical Page number |
TLB

Still 2 memory accesses

Save one memory access

TLB, Caches, Main Memory, Disk