Sudhanva Gurumurthi

Mailing Address: Ask via email
Website: http://www.cs.virginia.edu/~gurumurthi

Phone: Ask via email
Email: gsudhanva@gmail.com
Citizenship: United States of America

Technical Interests

I work in the fields of computer architecture, systems design, and warehouse scale computing. My interests include both engineering and business aspects of developing and delivering new technologies and capabilities. Technical areas I have worked on include:

- Data center design and operations
- Cloud and exascale computing
- Memory technologies and systems
- Resiliency and reliability of processors and large-scale systems
- Energy-efficient design

Education

PhD - Computer Science and Engineering 2000-2005
Dissertation: Power Management of Enterprise Storage Systems
Advisor - Anand Sivasubramaniam
Pennsylvania State University, University Park, PA, USA

Bachelor of Engineering - Computer Science and Engineering 1996-2000
College of Engineering Guindy, Anna University, Chennai, India

Current Employment

- **Advanced Micro Devices (AMD)**
  AMD Research
  Austin, TX, USA
  Principal Member of the Technical Staff: September 2016-Present

- **University of Virginia**
  Department of Computer Science
  Charlottesville, VA, USA
  Visiting Associate Professor: August 2014-Present

Employment History

- **International Business Machines (IBM)**
  Cloud Innovation Lab
  Austin, TX, USA
  Cloud Operations Architect and Manager: January 2016-September 2016
  Senior Data Center Engineer: August 2015-December 2015

  Work Highlights
  I was a technical leader and a manager in the IBM Cloud Innovation Lab, whose goal is to build a large-scale, next-generation IaaS cloud from the ground up. I served as the lead operations architect of this cloud. My duties and accomplishments include:

  - Design and delivery of OSS and BSS systems and processes, including data center operations, automation for efficient and reliable at-scale operations, support models and team design for both the cloud customers and operators, and offering management.
  - Bringing together DevOps squads within the Cloud Innovation Lab and others parts of the IBM Cloud division for the OSS and BSS integration of this IaaS platform into the overall IBM Cloud portfolio.
  - Recruiting and managing talent across different squads in Austin.

- **Advanced Micro Devices (AMD)**
  AMD Research
  Boxborough, MA, USA
  Senior Member of the Technical Staff: August 2012-July 2015

  Work Highlights

  - I built and led a talented team that defined and drove research into resiliency and reliability. The research carried out by this team included the development of new reliability techniques, RAS design methodologies and tools, and field studies of large system deployments. This work influenced product development in AMD, enhanced customer engagement, grew AMD's patent portfolio in RAS, and yielded publications at top peer-reviewed venues.
  - Provided guidance to R&D groups within the company and engaged in customer interactions related to emerging memory technologies.
  - Initiated and lead an effort to establish a research program in AMD in India.
  - Served as the technical lead for reliability in the US Department of Energy funded Exascale FastForward, FastForward2, and DesignForward2 contracts.

- **University of Virginia**
  Department of Computer Science
  Charlottesville, VA, USA
  - **Associate Professor (with tenure): August 2011-August 2014**
  - **Assistant Professor: August 2005-August 2011**

- **Intel Corporation**
  Hudson, MA, USA
  Graduate Intern: February-August 2004

  Work Description
  Designed and prototyped a distributed software infrastructure called *SEMA* for collecting and analyzing failure data from a large pool of systems. This project subsequently won the *Intel Divisional Recognition Award* and the *Intel Achievement Award.*

- **IBM Research**
  Austin, TX, USA
  Technical Co-Op: May-August 2003

  Work Description
  Developed a main memory system simulator for IBM p-Series™ servers and carried out a pathfinding study for future server memory system designs.

- **Pennsylvania State University**
  Department of Computer Science and Engineering
  University Park, PA, USA
  - **Research Assistant: 2001-2005**
  - **Teaching Assistant: 2000-2001**

Industry Consulting

- **Intel Corporation**
  Hudson, MA, USA
  Faculty Consultant: February 2008-July 2010

  Work Description
  Worked on refinements to runtime AVF predictors (originally developed by my research group at the University of Virginia) and evaluated feasibility of implementing this technology in x86 cores. Defined and contributed to a project on architecture support for improving reliability of accelerator-based platforms.

Awards/Honors

- IBM Manager's Choice Award, 2015
  (This award is conferred by managers to their direct reports who have demonstrated outcomes based on IBM values and practices.)
- AMD Innovation Fund Award, 2014
  (This award funds the development of select, innovative engineering projects that have the potential to benefit AMD, end-users, and/or society at large.)
- ACM Senior Member, 2011
  (This recognizes ACM members with "at least 10 years of professional experience who have demonstrated performance that sets them apart from their peers through technical leadership, and technical or professional contributions".)
- IEEE Senior Member, 2010
  (Fewer than 8% of the IEEE's 400,000 members hold this membership grade, which "recognizes significant professional technical accomplishment.")
- My group's research on energy-efficient storage highlighted in the National Science Foundation Budget Request to US Congress, 2009
- Paper selected for IEEE Micro Top Picks from the Computer Architecture Conferences, 2009
  (Top Picks recognizes "the most industry relevant and significant papers in computer architecture" in a given year.)
- NSF CAREER Award, 2007
  (This is the National Science Foundation's most prestigious award for junior faculty members)
- Nominated by Penn State for the ACM Doctoral Dissertation Award, 2005
  (One nomination per university)
- CSE Research Assistant Award, 2004
  (Four awarded per year for outstanding research in Computer Science and Engineering)

- Robert M. Owens Memorial Scholarship, 2003
  (One awarded per year for outstanding research in computer systems)
- Paper selected for the VLDB Journal Special Issue on the Best Papers of VLDB 2001

Selected Press Coverage and External Articles

- "Chipmaker AMD plans to super-size its processor", ZDNet, August 5, 2015.
- "AMD's Exascale Strategy Hinges on Heterogeneity", HPCwire, July 29, 2015.
- "Disks: how hot is too hot?", Storage Mojo, May 30, 2014.
- "HDD Warming: Global Data Threat?", ZDNet, May 14, 2014.
- "Elevation Plays a Role in Memory Error Rates", Slashdot, November 22, 2013.
- "Slower Disk Drives Could Slash Data Centre Power", TechWeek Europe, August 2011.
- "A Preview of Future Disk Drives", MIT Technology Review, June 13, 2011.
- "2010 Yearbook recognizes 25 famous locals you may not have heard of", C-Ville Weekly, April 20, 2010.
- IEEE Micro Top Picks 2009 Paper featured in IEEE Computing Now - "Directions in Enterprise Data Storage Systems", March 2010.
- "U.Va. Venture Summit Tackles Energy Frontier and Big Questions", UVA Today, March 29, 2010.
- "UVa Venture Summit Aims to Find Funds for Researchers", Charlottesville Daily Progress, March 25, 2010.
- "Google Grant Helping Data Center Project", Charlottesville Daily Progress, February 10, 2010.
- "Google Funds 'Radical' Efficiency Research", Data Center Knowledge, February 10, 2010.
- "U.Va. Computer Science Professor Receives $1 Million Google Research Award to Study Energy Efficiency in Data Centers", UVA Today, February 10, 2010.
- "Google Awards $1 Million for Research Effort to Slash Energy Consumption in Internet Data Centers", Dr. Dobb's Journal, February 4, 2010.
- "Google Gives Millions of Dollars in Research Awards", CNET News, February 2, 2010.
- "Announcing Google's Focused Research Awards", Google Blog, February 2, 2010.
- Storage energy-efficiency research featured in NSF Fiscal Year 2010 Budget Request to the US Congress, May 7, 2009.
- "Google University Research Awards", Google Research Blog, January 28, 2009.
- "CAREER Award Enables Adaptive Active Storage Research", UVA Research News, November 7, 2007.

Publications

In total, my papers have been cited **2924 times.** My **h-index** is **27**. The citation data was obtained using Google Scholar™. *(Last updated in June 2017).*

Book

PCM Book'11 M. Qureshi, S. Gurumurthi, B. Rajendran, Phase Change Memory: From Devices to Systems, *Synthesis Lectures on Computer Architecture Series*, Editor: Mark D. Hill, Morgan and Claypool Publishers, December 2011.

Refereed Journal Papers

IEEE TPDS'16 B. Fang, K. Pattabiraman, M. Ripeanu, S. Gurumurthi, A Systematic Methodology for Evaluating the Error Resilience of GPGPU Applications, *IEEE Transactions on Parallel and Distributed Systems (Accepted)*.

IEEE Micro'15 M. Schulte, M. Ignatowski, G. Loh, N. Jayasena, S. Gurumurthi, B. Beckmann, G. Rodgers, W. Brantley, I. Paul, S. Reinhardt, Achieving Exascale Capabilities through Heterogeneous Computing, *IEEE Micro - Special Issue on Heterogeneous Computing*, July/August 2015.

IEEE CAL'14 S. Sankar, S. Gurumurthi, Soft Failures in Large Datacenters, *IEEE Computer Architecture Letters*, 13(2), pages 105-108, July 2014.
(Acceptance Rate: 24%)

IEEE TCAD'13 V. Mohan, T. Bunker, L. Grupp, S. Gurumurthi, M.R. Stan, S. Swanson, Modeling Power Consumption of NAND Flash Memories using FlashPower, *IEEE Transactions on Computer Aided Design*, 32(7), pages 1031-1044, July 2013.

ACM TOS'13 S. Sankar, M. Shaw, K. Vaid, S. Gurumurthi, Datacenter Scale Evaluation of the Impact of Temperature on Hard Disk Drive Failures, *ACM Transactions on Storage*, 9(2), pages 1-24, July 2013.

IEEE TVLSI'12 T. Siddiqua, S. Gurumurthi, Enhancing NBTI Recovery in SRAM Arrays through Recovery Boosting, *IEEE Transactions on Very Large Scale Integration Systems*, 20(4), pages 616-629, April 2012.

IEEE Micro'09 Top Picks S. Gurumurthi, S. Sankar, M.R. Stan, Using Intradisk Parallelism to Build Energy Efficient Storage Systems, *IEEE Micro Special Issue on Top Picks from the Computer Architecture Conferences of 2008*, 29(1), pages 50-61, January/February 2009.
(Acceptance Rate: 15%)

IEEE TC'09 S. Sankar, Y. Zhang, S. Gurumurthi, M.R. Stan, Sensitivity-Based Optimization of Disk Architecture, *IEEE Transactions on Computers*, 58(1), pages 69-81, January 2009.

ASME JEP'08 Y. Kim, J. Choi, A. Sivasubramaniam, S. Gurumurthi, Managing Thermal Emergencies in Disk-Based Storage Systems, *ASME Journal of Electronic Packaging*, 130(4), December, 2008.

IEEE Micro'06 S. Gurumurthi, Y. Kim, A. Sivasubramaniam, Using STEAM for Thermal Simulation of Storage Systems, *IEEE Micro - Special Issue on Computer Architecture Simulation and Modeling*, 26(4), pages 43-51, July, 2006.

ACM TOS'06 S. Gurumurthi, A. Sivasubramaniam, Thermal Issues in Disk Drive Design: Challenges and Possible Solutions, *ACM Transactions on Storage*, 2(1), pages 41-73, February, 2006.

IEEE'03 Computer S. Gurumurthi, A. Sivasubramaniam, M. Kandemir, H. Franke, Reducing Disk Power Consumption in Servers with DRPM, *IEEE Computer - Special Issue on Power-Aware and Temperature-Aware Computing*, 36(12), pages 59-66, December, 2003.

VLDB'02 Journal N. An, S. Gurumurthi, A. Sivasubramaniam, N. Vijaykrishnan, M. Kandemir, M.J. Irwin, Energy-Performance Trade-Offs for Spatial Access Methods on Memory Resident Data, *The VLDB Journal - Special Issue on Best Papers of VLDB 2001*, 11(3), pages 179-197, November, 2002.

Invited Journal Papers

IEEE Micro'09 S. Gurumurthi, Architecting Storage for the Cloud Computing Era, *IEEE Micro*, 29(6), pages 68-71, November/December, 2009.

ACM OSR'07 S. Gurumurthi, Should Disks be Speed Demons or Brainiacs? *ACM SIGOPS Operating Systems Review - Special Issue on File and Storage Systems*, 41(1), pages 33-36, January 2007.

Refereed Conference and Competitive Workshop Papers

DSN'16 B. Fang, Q. Lu, K. Pattabiraman, M. Ripeanu, S. Gurumurthi, ePVF: An Enhanced Program Vulnerability Factor Methodology for Holistic Resilience Analysis, *International Conference on Dependable Systems and Networks*, Toulouse, France, June 2016.
(Acceptance Rate: 22%)

IRPS'16 S. Li, V. Sridharan, S. Gurumurthi, S. Yalamanchili, Software-based Dynamic Reliability Management for GPU Applications, *International Reliability Physics Symposium*, Pasadena, CA, April 2016.

ASPLOS'15 V. Sridharan, N. DeBardeleben, S. Blanchard, K. Ferreira, J. Stearley, J. Shalf, S. Gurumurthi, Memory Errors in Modern Systems: The Good, The Bad, and the Ugly, *Proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems*, Istanbul, Turkey, March 2015.
(Acceptance Rate: 17%)

MICRO'14 M. Wilkening, V. Sridharan, D. Kaeli, S. Li, F. Previlon, S. Gurumurthi, Calculating Architectural Vulnerability Factors for Spatial Multi-Bit Transient Faults. *Proceedings of the International Symposium on Microarchitecture*, Cambridge, UK, December 2014.
(Acceptance Rate: 19%)

ISCA'14 J. Wadden, A. Lyashevsky, S. Gurumurthi, V. Sridharan, K. Skadron, Real-World Design and Evaluation of Compiler-Managed GPU Redundant Multithreading, *Proceedings of the International Symposium on Computer Architecture*, Minneapolis, MN, June 2014.
(Acceptance Rate: 18%)

CF'14 S. Sankar, D. Gauthier, S. Gurumurthi, Power Availability Provisioning in Large Data Centers, *Proceedings of ACM International Conference on Computing Frontiers*, Cagliari, Italy, June 2014.
(Acceptance Rate: 45%)

DATE'14 L. Bautista Gomez, F. Cappello, L. Carro, N. DeBardeleben, B. Fang, S. Gurumurthi, K. Pattabiraman, P. Rech, M. Sonza Reorda, GPGPUs: How to combine high computational power with high reliability, *Proceedings of the Design, Automation, and Test in Europe Conference*, Dresden, Germany, March 2014.
(Invited Paper)

ISPASS'14 B. Fang, K. Pattabiraman, M. Ripeanu, S. Gurumurthi, GPU-Qin: A Methodology for Evaluating the Error Resilience of GPGPU Applications, *Proceedings of the International Symposium on Performance Analysis of Systems and Software*, Monterey, CA, March 2014.
(Acceptance Rate: 33%)

SC'13 V. Sridharan, J. Stearley, N. DeBardeleben, S. Blanchard, S. Gurumurthi, Feng Shui of Supercomputer Memory - Positional Effects in DRAM and SRAM Faults, *Proceedings of the Supercomputing*, Denver, CO, November 2013.

(Acceptance Rate: 20%)

MASCOTS'13 L. Jiang, S. Gurumurthi, A Novel Simulation Methodology For Accelerating Reliability Assessment of SSDs, *Proceedings of the International Symposium on Modeling, Analysis, and Simulation of Computer and Telecommunication Systems*, San Francisco, CA, August 2013. *(Short Paper)*
(Acceptance Rate: 40%)

ICCAD'11 C.W. Smullen, A. Nigam, S. Gurumurthi, M.R. Stan, The STeTSiMS STT-RAM Simulation and Modeling System, *Proceedings of the International Conference on Computer-Aided Design*, San Jose, CA, November 2011.
(Acceptance Rate: 30%)

ISLPED'11 A. Nigam, C.W. Smullen, V. Mohan, E. Chen, S. Gurumurthi, M.R. Stan, Delivering on the Promise of Universal Memory for Spin Torque Transfer RAM (STT-RAM), *Proceedings of the International Symposium on Low-Power Electronics and Design*, Fukuoka, Japan, August, 2011.
(Acceptance Rate: 23%)

ISQED'11 T. Siddiqua, S. Gurumurthi, M.R. Stan, Modeling and Analyzing NBTI in the Presence of Process Variation, *Proceedings of the International Symposium on the Quality of Electronic Design*, Santa Clara, CA, March, 2011.
(Acceptance Rate: 52%)

HPCA'11 C.W. Smullen, V. Mohan, A. Nigam, S. Gurumurthi, M.R. Stan, Relaxing Non-Volatility for Fast and Energy-Efficient STT-RAM Caches, *Proceedings of the International Symposium on High-Performance Computer Architecture*, San Antonio, TX, February, 2011.
(Acceptance Rate: 19%)

IGCC'10 C.W. Smullen, J.S. Coffman, S. Gurumurthi, Accelerating Enterprise Solid-State Disks with Non-Volatile Merge Caching, *Proceedings of the IEEE International Green Computing Conference*, Chicago, IL, August 2010.
(Acceptance Rate: 30%)

ISVLSI'10 T. Siddiqua, S. Gurumurthi, Recovery Boosting: A Technique to Enhance NBTI Recovery in SRAM Arrays, *Proceedings of the IEEE Computer Society Annual Symposium on VLSI*, Lixouri Kefalonia, Greece, July 2010.
(Acceptance Rate: 33%)

HotStorage'10 V. Mohan, T. Siddiqua, S. Gurumurthi, M.R. Stan, How I Learned to Stop Worrying and Love Flash Endurance, *USENIX Workshop on Hot Topics in Storage and File Systems*, Boston, MA, June 2010.
(Acceptance Rate: 31%)

GLSVLSI'10 T. Siddiqua, S. Gurumurthi, A Multi-Level Approach to Reduce the Impact of NBTI on Processor Functional Units, *Proceedings of the Great Lakes Symposium on VLSI*, Providence, RI, pages 67-72, May 2010.
(Acceptance Rate: 18%)

DATE'10 V. Mohan, S. Gurumurthi, M.R. Stan, FlashPower: A Detailed Power Model for NAND Flash Memory, *Proceedings of the Design, Automation, and Test in Europe Conference*, Dresden, Germany, pages 502-507, March 2010.
(Acceptance Rate: 30%)

SEMITHERM'10 W. Huang, K. Skadron, S. Gurumurthi, R.J. Ribando, M.R. Stan, Exploring the Thermal Impact on Manycore Processor Performance, *Proceedings of the Annual Thermal Measurement, Modeling, and Management Symposium*, Santa Clara, CA, pages 191-197, February 2010.

SEMITHERM'10 W. Huang, K. Skadron, S. Gurumurthi, R.J. Ribando, M.R. Stan, Interaction of Scaling Trends in Processor Architecture and Cooling, *Proceedings of the Annual Thermal Measurement, Modeling, and Management Symposium*, Santa Clara, CA, pages 198-204, February 2010.

MASCOTS'09 T. Siddiqua, S. Gurumurthi, Balancing Soft Error Coverage with Lifetime Reliability in Redundantly Multithreaded Processors, *Proceedings of the International Symposium on Modeling, Analysis, and Simulation of Computer and Telecommunication Systems*, London, UK, pages 99-110, September, 2009.
(Acceptance Rate: 20%)

ISPASS'09 W. Huang, K. Skadron, S. Gurumurthi, R. Ribando, M.R. Stan, Differentiating the Roles of IR Measurement and Simulation for Power and Temperature-Aware Design, *Proceedings of the International Symposium on Performance Analysis of Systems and Software*, Boston, MA, pages 1-10, April 2009.
(Acceptance Rate: 28%)

MASCOTS'08 S. Sankar, S. Gurumurthi, M.R. Stan, Sensitivity Based Power Management of Enterprise Storage Systems, *Proceedings of the International Symposium on Modeling, Analysis, and Simulation of Computer and Telecommunication Systems*, Baltimore, MD, September 2008.
(Acceptance Rate: 38%)

ISCA'08 S. Sankar, S. Gurumurthi, M. Stan, Intra-Disk Parallelism: An Idea Whose Time Has Come, *Proceedings of the International Symposium on Computer Architecture*, Beijing, China, pages 303-314, June 2008.
(Acceptance Rate: 14%)

CF'08 C.W. Smullen, S.R. Tarapore, S. Gurumurthi, P. Ranganathan, M. Uysal, Active Storage Revisited: The Case for Power and Performance Benefits for Unstructured Data Processing Applications, *Proceedings of ACM International Conference on Computing Frontiers*, Ischia, Italy, pages 293-304, May, 2008.
(Acceptance Rate: 27%)

ISCA'07 K.R. Walcott, G. Humphreys, S. Gurumurthi, Dynamic Prediction of Architectural Vulnerability From Microarchitectural State, *Proceedings of the International Symposium on Computer Architecture*, San Diego, CA, pages 516-527, June 2007.
(Acceptance Rate: 22%)

DAC'07 Y. Zhang*, S. Gurumurthi, M. Stan, SODA: Sensitivity Based Optimization of Disk Architecture, *Proceedings of the Design Automation Conference*, San Diego, CA, pages 865-870, June 2007.
(Acceptance Rate: 23%)

THETA'07 Y. Kim, J. Choi, A. Sivasubramaniam, S. Gurumurthi, Graceful Operation of Disk Drives Under Thermal Emergencies, *Proceedings of the International Conference on Thermal Issues in Emerging Technologies Theory and Application*, Cairo, Egypt, pages 119-125, January 2007.

ASPLOS'06 A. Parashar, S. Gurumurthi, A. Sivasubramaniam, SlicK: Slice-Based Locality Exploitation for Efficient Redundant Multithreading, *Proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems*, San Jose, CA, pages 95-105, October 2006.
(Acceptance Rate: 24%)

ITHERM'06 S. Gurumurthi, The Need for Temperature-Aware Storage Systems, *Proceedings of the Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*, San Diego, CA, pages 387-394, May 2006.
(Acceptance Rate: 61%)

MSST'06 N. Paul*, S. Gurumurthi, D. Evans, Thermal Attacks on Storage Systems, *Proceedings of the NASA Goddard/IEEE Conference on Mass Storage Systems and Technologies*, College Park, MD, pages 143-151, May 2006.
(Acceptance Rate: 50%)

HPCA'06 Y. Kim, S. Gurumurthi, A. Sivasubramaniam, Understanding the Performance-Temperature Interactions in Disk I/O of Server Workloads, *Proceedings of the International Symposium on High Performance Computer Architecture*, Austin, TX, pages 179-189, February 2006.
(Acceptance Rate: 15%)

ISCA'05 S. Gurumurthi, A. Sivasubramaniam, V.K. Natarajan, Disk Drive Roadmap from the Thermal Perspective: A Case for Dynamic Thermal Management, *Proceedings of the International Symposium on Computer Architecture*, Madison, WI, pages 38-49, June 2005.
(Acceptance Rate: 23%)

ISCA'04 A. Parashar, S. Gurumurthi, A. Sivasubramaniam, A Complexity-Effective Approach to ALU Bandwidth Enhancement for Instruction-Level Temporal Redundancy, *Proceedings of the International Symposium on Computer Architecture*, Munich, Germany, pages 376-386, June 2004.
(Acceptance Rate: 14%)

DSN'03 W. Zhang, S. Gurumurthi, M. Kandemir, A. Sivasubramaniam, ICR: In-Cache Replication for Enhancing Data Cache Reliability, *Proceedings of the International Conference on Dependable Systems and Networks*, San Francisco, CA, pages 291-300, June 2003.
(Acceptance Rate: 21%)

ISCA'03 S. Gurumurthi, A. Sivasubramaniam, M. Kandemir, H. Franke, DRPM: Dynamic Speed Control for Power Management in Server Class Disks, *Proceedings of the International Symposium on Computer Architecture*, San Diego, CA, pages 169-179, June 2003.
(Acceptance Rate: 20%)

ISPASS'03 S. Gurumurthi, J. Zhang, A. Sivasubramaniam, M. Kandemir, H. Franke, N. Vijaykrishnan, M.J. Irwin, Interplay of Energy and Performance for Disk Arrays Running Transaction Processing Workloads, *Proceedings of the International Symposium on Performance Analysis of Systems and Software*, Austin, TX, pages 123-132, March 2003.
(Acceptance Rate: 35%)

IPDPS'03 S. Gurumurthi, N. An, A. Sivasubramaniam, N. Vijaykrishnan, M. Kandemir, M.J. Irwin, Energy-Performance Considerations in Work Partitioning for Mobile Spatial Queries, *Proceedings of the International Parallel and Distributed Processing Symposium*, Nice, France, April 2003.
(Acceptance Rate: 29%)

HPCA'02 S. Gurumurthi, A. Sivasubramaniam, M.J. Irwin, N. Vijaykrishnan, M. Kandemir, T. Li, L.K. John, Using Complete Machine Simulation for Software Power Estimation: The SoftWatt Approach, *Proceedings of the International Symposium on High Performance Computer Architecture*, Boston, MA, pages 141-150, February 2002.
(Acceptance Rate: 20%)

VLDB'01 N. An, A. Sivasubramaniam, N. Vijaykrishnan, M. Kandemir, M.J. Irwin, S. Gurumurthi, Analyzing Energy Behavior of Spatial Access Methods for Memory-Resident Data, *Proceedings of the International Conference on Very Large Data Bases*, Rome, Italy, pages 411-420, September 2001.
(Acceptance Rate: 17%)

Refereed Workshop Papers

SELSE'15 S. Li, V. Sridharan, S. Gurumurthi, S. Yalamanchili, Software-based Dynamic Reliability Management for GPU Applications. *IEEE Workshop on Silicon Errors in Logic - System Effects*, Austin, TX, March 2015.

SELSE'15 F. Previlon, M. Wilkening, V. Sridharan, D. Kaeli, S. Gurumurthi, Examining the Impact of ACE Interference on Multi-Bit AVF Estimates. *IEEE Workshop on Silicon Errors in Logic - System Effects*, Austin, TX, March 2015.

FTXS'14 B. Fang, K. Pattabiraman, M. Ripeanu, S. Gurumurthi, Evaluating the Error Resilience of Parallel Programs, *Fault Tolerance for HPC at eXtreme Scale Workshop (Held in conjunction with DSN)*, Atlanta, GA, June 2014.

SELSE'14 N. DeBardeleben, S. Blanchard, V. Sridharan, S. Gurumurthi, J. Stearley, K. Ferreira, Extra Bits on SRAM and DRAM Errors - More Data from the Field, *IEEE Workshop on Silicon Errors in Logic - System Effects*, Palo Alto, CA, March 2014.

GPUDEP'14 S. Li, V. Sridharan, S. Gurumurthi, S. Yalamanchili, Software-Based Techniques for Reducing the Vulnerability of GPU Applications, *International Workshop on Dependable GPU Computing (Held in Conjunction with DATE)*, Dresden, Germany, March 2014.

MODSIM'13 B. Beckmann, Y. Eckert, M. Arora, S. Gurumurthi, S. Reinhardt, V. Sridharan, A Comprehensive Timing, Power, Thermal, and Reliability Model for Exascale Node Architectures, *DOE Workshop on Modeling and Simulation of Exascale Systems and Applications*, Seattle, WA, September 2013.
(Acceptance Rate: 45%)

SELSE'13 T. Siddiqua, A. Papathanasiou, A. Biswas, S. Gurumurthi, Analysis and Modeling of Memory Errors from Large-Scale Field Data Collection, *IEEE Workshop on Silicon Errors in Logic - System Effects*, Palo Alto, CA, March 2013.

SELSE'13 H. Jeon, M.Wilkening, V. Sridharan, S. Gurumurthi, G. Loh, Architecturual Vulnerability Modeling and Analysis of Integrated Graphics Processors, *IEEE Workshop on Silicon Errors in Logic - System Effects*, Palo Alto, CA, March 2013.

SELSE'09 A. Biswas, N. Soundararajan, S.S. Mukherjee, S. Gurumurthi, Quantized AVF: A Means of Capturing Vulnerability Variations over Small Windows of Time, *IEEE Workshop on Silicon Errors in Logic - System Effects*, Palo Alto, CA, March 2009.

SELSE'09 T. Siddiqua, S. Gurumurthi, NBTI-Aware Dynamic Instruction Scheduling, *IEEE Workshop on Silicon Errors in Logic - System Effects*, Palo Alto, CA, March 2009.

SELSE'09 B.C. Sutton, S. Gurumurthi, Single-Threaded Mode AVF Prediction During Redundant Execution, *IEEE Workshop on Silicon Errors in Logic - System Effects*, Palo Alto, CA, March 2009.

MoBS'08 S.R. Tarapore, C.W. Smullen, S. Gurumurthi, MIDAS: An Execution-Driven Simulator for Active Storage Architectures, *Proceedings of the Workshop on Modeling, Benchmarking, and Simulation (Held in conjunction with ISCA)*, Beijing, China, June 2008.
(Acceptance Rate: 60%)

CATARS'08 N. George*, J. Lach, S. Gurumurthi, Towards Transient Fault Tolerance for Heterogeneous Computing Platforms, *Proceedings of the Workshop of Compiler and Architectural Techniques for Application Reliability and Security (Held in conjunction with DSN)*, Anchorage, AK, June 2008.

SNAPI'07 C.W. Smullen, S.R. Tarapore, S. Gurumurthi, A Benchmark Suite for Unstructured Data Processing, *Proceedings of the International Workshop on Storage Network Architecture and Parallel I/Os (Held in conjunction with MSST)*, San Diego, CA, September 2007.
(Acceptance Rate: 35%)

HPCRI'05 S. Gurumurthi, A. Parashar, A. Sivasubramaniam, SOS: Using Speculation for Memory Error Detection, *Proceedings of the Workshop on High Performance Computing Reliability Issues (Held in conjunction with HPCA)*, San Francisco, CA, February 2005.

CAECW'05 V. Natarajan, S. Gurumurthi, A. Sivasubramaniam, Is Traditional Power Management + Prefetching == DRPM for Server Disks?, *Proceedings of the Workshop on Computer Architecture Evaluation Using Commericial Workloads (Held in conjunction with HPCA)*, San Francisco, CA, February 2005.

Book Chapters

SPRINGER'18 V. Sridharan, S. Gurumurthi, Resilience Proportionality - A Paradigm for Efficient and Reliable System Design, *Manufacturable and Dependable Multicore Architectures at Nanoscale*, Editors: Marco Ottavi, Dimitris Gizopoulos and Salvatore Pontarelli, Springer, 2018.

CRC'12 Y. Kim, S. Gurumurthi, A. Sivasubramaniam, Dynamic Thermal Management for High-Performance Storage Systems, *Handbook of Energy-aware and Green Computing*, Editors: Ishfaq Ahmad and Sanjay Ranka, CRC Press, January 2012.

WILEY'12 S. Gurumurthi, A. Sivasubramaniam, Energy Efficient Storage Systems for Data Centers, *Energy Efficient Distributed Computing Systems*, Editors: Albert Zomaya and Young Choon Lee, Wiley Publishers, August 2012.

Unpublished Technical Reports

TR-12 V. Mohan, S. Sankar, S. Gurumurthi, reFresh SSDs - Enabling High Endurance, Low Cost Flash in Datacenters, Department of Computer Science, University of Virginia Technical Report CS-2012-05, May 2012.

Other Publications

PRDC'13 B. Fang, K. Pattabiraman, M. Ripeanu, S. Gurumurthi, Characterizing and Understanding the Error Resilience of GPGPU Applications, *IEEE Pacific Rim International Symposium on Dependable Computing*, December 2013. (Poster)

FMS'12 V. Mohan, S. Sankar, S. Gurumurthi, reFresh SSDs - Enabling High Endurance, Low Cost Flash in Datacenters, Flash Memory Summit, August 2012. (Abstract)

HPTS'11 S. Gurumurthi, Memory is the New Disk, International Workshop on High-Performance Transaction Systems, October 2011. (Abstract)

NVMW'11 C.W. Smullen, S. Gurumurthi, Designing with STT-RAM: From Disks to Dies, Non-Volatile Memories Workshop, March 2011. (Abstract)

(Acceptance Rate: 51%)

NVMW'11 V.Mohan, S. Gurumurthi, Tools for Architecture-level Design and Analysis of Flash Memory Systems, Non-Volatile Memories Workshop, March 2011. (Poster)

GHC'09 T. Siddiqua, S. Gurumurthi, Dynamic NBTI Management in Multicore Processor, Grace Hopper Celebration of Women in Computing Conference, September, 2009.
(Acceptance Rate: 10% of Submitted Abstracts; First Place Winner of the ACM Student Research Competition at GHC)

USENIX Security'06 A. Felt*, N. Paul*, D. Evans, S. Gurumurthi, Taking Virus Detection to the Next Level (Down), *USENIX Security Symposium - Work-in-Progress Abstract*, July 2006.

COBASSA'05 N. Paul*, S. Gurumurthi, D. Evans, Towards Disk-Level Malware Detection, *Proceedings of the Workshop on Code Based Software Security Assessment (Held in conjunction with WCRE)*, November 2005.

DAC'02 S. Gurumurthi, Energy Efficient Software Design: The Resource-Constrained and Resource-Rich Perspectives, *Design Automation Conference - PhD Forum Poster*, June 2002.

Patents

Issued Patents

1. S. Gurumurthi, V. Sridharan, Using Redundant Transactions to Verify the Correctness of Program Code Execution, 9,448,933, September 2016. (Filed by AMD)
2. V. Sridharan, M. Wilkening, S. Gurumurthi, Determining the Vulnerability of Multi-Threaded Program Code to Soft Errors, U.S. Patent (Number: 9,292,418), March 2016. (Assignee: AMD)
3. S. Gurumurthi, V. Sridharan, Signature Based Store Checking Buffer, U.S. Patent (Number: 9,047,192), June 2015. (Assignee: AMD)
4. S. Gurumurthi, V. Sridharan, Hardware Based Redundant Multi-Threading Inside a GPU for Improved Reliability, U.S. Patent (Number: 9,026,847), May 2015. (Assignee: AMD)
5. S. Gurumurthi, A. Biswas, J. Emer, S.S. Mukherjee, Detecting Errors in Directory Entries, U.S. Patent (Number: 7,475,321), January 2009. (Assignee: Intel)

In-Flight US Patent Applications and Filing Dates

1. S. Che, S. Gurumurthi, M. Boyer, Infrastructure to Support Accelerator Computation Models for Active Storage, 14/709,915, May 2015 (Filed by AMD)
2. A. Lyashevsky, S. Gurumurthi, V. Sridharan, Software only Inter-Compute Unit Redundant Multi-Threading for GPUs, 13/920574, June 2013. (Filed by AMD)
3. A. Lyashevsky, S. Gurumurthi, V. Sridharan, Software only Intra-Compute Unit Redundant Multi-Threading for GPUs, 13/920524, June 2013. (Filed by AMD)
4. D. Evans, A. Felt*, N. Paul*, S. Gurumurthi, Method, System and Computer Program Product for Behavioral Malware Detection, Analysis, and Response, 12/445889, October 2007. (Filed by the University of Virginia)

External Research Funding

- *A Data-Centric Approach to Energy Proportionality*
  Sponsor: Google Energy Efficiency and Proportionality in Datacenter-class Computing grant
  Amount: $1,500,000
  Date: 3 Years
  Co-PI; PIs: Ricardo Bianchini (Rutgers) and Frederic Chong (UCSB). Other CO-PIs: Thomas Wenisch (Michigan)
  (25% of the Funds Allocated to Each PI)
- *Energy-Efficient Storage Architectures for Data Centers*
  Sponsor: Google Research Award
  Amount: $80,000
  Date: 01/01/2009
  Sole PI
- *Reliability Sensors at the Circuit and Architecture Levels*
  Sponsor: Intel Corporation
  Amount: $70,000
  Dates: (First Payment: 09/01/2008; Second payment: 6/10/2009; Renewable Yearly)
  Co-PI; PI: Mircea Stan (ECE) (50% of the Funds Allocated to Each PI)
- *Research Experiences for Undergraduates Supplement*
  Sponsor: National Science Foundation
  (Supplement to *CRI: Comprehensive, Industry-Strength System-Level Thermal Modeling*)
  Amount: $12,763
  Dates: 05/01/2008 - 04/30/2009
  Co-PI; PI: Kevin Skadron. Other Co-PIs: Mircea Stan (ECE) and Robert J. Ribando (MAE) (25% of the Funds Allocated to Each PI)
- *Novel Disk Drive Architectures for Efficient Processing of Unstructured Datasets*
  Sponsor: Google Research Award
  Amount: $40,000
  Date: 12/21/2007
  Sole PI
- *Storage-Centric Architectures*
  Sponsor: Hewlett-Packard Company
  Amount: $35,000
  Date: 06/29/2007
  Sole PI
- *Research Experiences for Undergraduates Supplement*
  Sponsor: National Science Foundation
  (Supplement to *CT-ISG: Disk-Level Malware Detection and Response*)
  Amount: $12,000
  Dates: 06/01/2007 - 07/31/2007
  Co-PI; PI: David Evans (50% of the Funds Allocated to Each PI)
- *Research Experiences for Undergraduates Supplement*
  Sponsor: National Science Foundation
  (Supplement to *CAREER: Architectural Techniques and Tools for Adaptive Active Storage Systems*)
  Amount: $12,000
  Dates: 04/01/2007 - 03/31/2008
  Sole PI
- *CAREER: Architectural Techniques and Tools for Adaptive Active Storage Systems (Award #: 0643925)*
  Sponsor: National Science Foundation
  Amount: $400,000
  Dates: 04/01/2007 - 03/31/2012
  Sole PI

- *CT-ISG: Disk-Level Malware Detection and Response (Award #: 0627527)*
  Sponsor: National Science Foundation
  Amount: $400,000
  Dates: 09/01/2006 - 08/31/2009
  Co-PI; PI: David Evans (50% of the Funds Allocated to Each PI)
- *Processor Support for Platform Level Security*
  Sponsor: Intel Corporation
  Amount: $83,456.00
  Dates: (First Payment: 07/27/2006; Second Payment: 05/15/2007)
  Sole PI
- *CRI: Comprehensive, Industry-Strength System-Level Thermal Modeling (Award #: 0551630)*
  Sponsor: National Science Foundation
  Amount: $485,000
  Dates: 05/15/2006 - 04/30/2009
  Co-PI; PI: Kevin Skadron. Other Co-PIs: Mircea Stan (ECE) and Robert J. Ribando (MAE) (25% of the Funds Allocated to Each PI)

Invited Technical Panels and Meetings

- Workshop on Silicon Errors in Logic - System Effects (SELSE) panel: "Resilience and Probabilistic Computing", Austin, TX, March 2016.
- International Workshop on Dependable GPU Computing panel: "Faults in CPUs and GPUs: Same or Different Problems? Same or Different Solutions", Dresden, Germany, March 2014. (Held in conjunction with DATE 2014)
- Invited Participant, NSF Workshop on Cross-Layer Power Optimization and Management (CPOM), Los Angeles, CA, February 2012.
- Workshop on Architectural Concerns in Large Datacenters (ACLD) panel: "Debate: The Future of Persistent Storage in a Datacenter", Saint-Malo, France, June 2010. (Held in conjunction with ISCA 2010)
- University of Virginia Venture Summit, Regional Energy Initiatives and Opportunities panel, Charlottesville, VA, March 2010.
- Invited speaker, "Towards Hybrid Enterprise Storage Systems", Storage Networking Industry Association (SNIA) Solid-State Devices (SSD) Forum Meeting, SNIA Summer Symposium, San Jose, CA, July 2008.
- Invited Attendee, Google Faculty Summit, Mountain View, CA, July 2008.

Talks

Invited Conference Talks

- "Processor Design for Exascale Computing", Design Automation Conference (DAC), Austin, TX, June 2017.
- "Exascale Computing Research at AMD", Supercomputing (SC16), Salt Lake City, UT, November 2016.
- "Resilience at Scale: Insights and Opportunities", International Conference on Computer-Aided Design (ICCAD), Austin, TX, November 2015.
- **KEYNOTE:** "Failures in Large-Scale Systems: Insights from the Field", Fault Tolerance for HPC at Extreme Scale Workshop (FTXS), Portland, OR, June 2015.
- "The Fault Environment Unveiled", Salishan Conference on High Speed Computing, Gleneden Beach, OR, April 2015.
- "GPGPU Reliability - Challenges and Research Opportunities", International Workshop on Dependable GPU Computing, Dresden, Germany, March, 2014. (Held in conjunction with DATE 2014)
- "Towards Energy-Efficient Data Centers", nanoSTAR Spring Symposium, University of Virginia, Charlottesville, VA, May 2010.

- **KEYNOTE:** "The Role of Storage Class Memory in Future Hardware Platforms: Challenges and Opportunities", Workshop on the Use of Emerging Storage and Memory Technologies (WEST), Bangalore, India, January 2010. (Held in conjunction with HPCA 2010)
- **ACADEMIC INNOVATION SPOTLIGHT TALK:** "Intra-Disk Parallelism: A Green Storage Solution for Data Centers", Storage Developer Conference, Santa Clara, CA, September 2008.
- "Towards Hybrid Enterprise Storage Systems", SNIA Summer Symposium, San Jose, CA, July 2008.

Invited Colloquium Talks

- "Processor Design for Exascale Computing", University of Texas at San Antonio, San Antonio, TX, September 2017.
- "Resilience at Scale: Insights and Opportunities", University of Texas at Austin, Austin, TX, November 2015.
- "Resiliency and Reliability for Accelerator-Based Exascale Systems", Ghent University, Ghent, Belgium, May 2015.
- "Resiliency and Reliability for Accelerator-Based Exascale Systems", Georgia Institute of Technology, Atlanta, GA, April 2015.
- "Resiliency and Reliability for Accelerator-Based Exascale Systems", Harvard University, Cambridge, MA, October 2014.
- "Extreme-Scale Computing Research in AMD", Supercomputing Education and Research Centre, Indian Institute of Science, Bangalore, India, February 2014.
- "Reliability Challenges for the Exascale Era", Vellore Institute of Technology, Chennai, India, September 2013.
- "Reliability Challenges for the Exascale Era", College of Engineering Guindy, Anna University, Chennai, India, September 2013.
- "Reliability Challenges for the Exascale Era", University of Virginia, Charlottesville, VA, May 2013.
- "Non-Volatile Memory Hierarchies", AMD Research, Bellevue, WA, February 2012.
- "Non-Volatile Memory Hierarchies", Intel Corporation, Hudson, MA, September 2011.
- "Non-Volatile Memory Hierarchies", Microsoft Research, Redmond, WA, June 2011.
- "Energy-Efficient Server Memory Hierarchies", NetApp Webinar, February 2011.
- "Architecting Energy Efficient Storage for Data Centers", IBM T.J. Watson Research Center, Hawthorne, NY, July 2010.
- "Efficient Processor Fault Tolerance", Duke University, Durham, NC, May 2010.
- "Efficient Processor Fault Tolerance", University of Michigan, Ann Arbor, MI, April 2010.
- "Efficient Processor Fault Tolerance", University of California, San Diego, CA, April 2010.
- "Efficient Processor Fault Tolerance", University of Wisconsin, Madison, WI, April 2010.
- "Efficient Processor Fault Tolerance", Harvard University, Cambridge, MA, April 2010.
- "Efficient Soft Error Protection for Microprocessors", HP R&D Engineering Seminar - Computer Architecture Technologist series, March 2010.
- "Efficient Processor Fault Tolerance", University of Illinois, Urbana-Champaign, IL, February 2010.
- "Intra-Disk Parallelism: A Green Storage Architecture for Data Centers", Indian Institute of Science, Bangalore, India, January 2010.
- "Intra-Disk Parallelism: A Green Storage Solution for Data Centers", Cambridge University, Cambridge, UK, September 2009.
- "Intra-Disk Parallelism: A Green Storage Solution for Data Centers", University of California at Santa Cruz, Santa Cruz, CA, September 2008.
- "Intra-Disk Parallelism", Google, Mountain View, CA, July 2008.

- "Disk-Level Behavioral Malware Detection", Intel Corporation, Hillsboro, OR, August 2007.
- "Disk-Level Behavioral Malware Detection", Georgia Institute of Technology, Atlanta, GA, April 2007.
- "Disk-Level Behavioral Malware Detection", VMWare, Palo Alto, CA, March 2007.
- "Power Management of Enterprise Storage Systems", HP Labs, Palo Alto, CA, October 2006.
- "Processor Support for Platform Level Security", Intel Corporation, Hudson, MA, September 2006.
- "Virtual Redundant Threading", University of Virginia, Charlottesville, VA, April 2005.
- "Power Management of Enterprise Storage Systems", University of Virginia, Charlottesville, VA, April 2005.
- "Power Management of Enterprise Storage Systems", Purdue University, West Lafayette, IN, April 2005.
- "Power Management of Enterprise Storage Systems", Rutgers University, New Brunswick, NJ, April 2005.
- "Virtual Redundant Threading", University of Rochester, Rochester, NY, March 2005.
- "Power Management of Enterprise Storage Systems", University of Rochester, Rochester, NY, March 2005.
- "Virtual Redundant Threading", University of Massachusetts – Amherst, Amherst, MA, February 2005.
- "Power Management of Enterprise Storage Systems", University of Massachusetts – Amherst, Amherst, MA, February 2005.
- "Power Management of Enterprise Storage Systems", University of Minnesota – Twin-Cities, Minneapolis, MN, February 2005.
- "Power Management of Enterprise Storage Systems" Princeton University, Princeton, NJ, February 2005.
- "Thermal Issues in Disk Drive Design: Challenges and Solutions", Seagate Research Center, Pittsburgh, PA, March 2005.
- "A Complexity-Effective Approach to ALU Bandwidth Enhancement for Instruction-Level Temporal Redundancy", Intel Corporation, Hudson, MA, June 2004.
- "Power-Aware Design of the Main-Memory System in Servers", IBM Research, Austin, TX, August 2003.

Research Interns Mentored in Industry

- **AMD**
  - Fritz Previlon, Northeastern University, May-July 2015
  - Charu Kalra, Northeastern University, February-July 2015
  - Brandon Reagen, Harvard University, January-May 2015
  - Si Li, Georgia Institute of Technology, August 2013-May 2014
  - Jinsuk Chung, University of Texas at Austin, May-August 2013
  - Jack Wadden, University of Virginia, January-July 2013
  - Mark Wilkening, Northeastern University, January-August 2013; January-June 2015

Post-Doctoral Scholars and Research Contractors Mentored in Industry

- **AMD**
  - Taniya Siddiqua, January-July 2015
  - Daniel Lowell, July 2013-December 2014 (Promoted to full-time at AMD in January 2015)

Graduate Students Mentored in Academia

Graduated Doctoral Students

- Sriram Sankar
  - PhD Completed in Spring 2014
  - Dissertation Title: Impact of Datacenter Infrastructure on Server Availability - Characterization, Management, and Optimization
  - First Employment: Microsoft
- Taniya Siddiqua
  - PhD Completed in Fall 2012
  - Dissertation Title: A Multi-Level Approach to NBTI Mitigation in Processors
  - First Employment: Intel
- Clinton Wills Smullen, IV
  - PhD Completed in Fall 2011
  - Dissertation Title: Designing Giga-Scale Memory Systems with STT-RAM
  - First Employment: Google

Graduated Masters Students

- Luyao Jiang
  - MS, May 2013
  - Thesis Title: *Accelerating Reliability Simulation of NAND Flash based Solid State Drives*
  - First Employment: Google
- Abhishek Rawat
  - MCS, August 2011
  - First Employment: IBM
- Vidyabhushan Mohan
  - MS, May 2010
  - Thesis Title: *Modeling the Physical Characteristics of NAND Flash Memory*
  - First Employment: Sandisk
- Blake Carey Sutton
  - MCS, May 2009
  - First Employment: Google
- Kristen Rachelle Walcott
  - MCS, May 2007
  - First Employment: PhD program at UVa

Doctoral Committees

- Jack Wadden *(CS)*
  Advisor: Kevin Skadron
- Tanima Dey (*CS*)
  PhD Defense Completed in July 2014
  Dissertation : ReSense: A Unified Framework for Improving Performance and Reliability in Multicore Architectures
  Advisors: Mary Lou Soffa and Jack Davidson

- Ming Mao (*CS*)
  PhD Defense Completed in December 2012
  Dissertation Title: Cloud Auto-Scaling with Deadline and Budget Constraints
  Advisor: Marty Humphrey
- Kristen Rachelle Walcott (*CS*)
  PhD Defense Completed in May 2012
  Dissertation Title: Exploiting Hardware Mechanisms and Multicore Technology in Software Testing
  Advisor: Mary Lou Soffa
- Michael Boyer (*CpE*)
  PhD Proposal Completed in April 2012
  Dissertation Title: Dynamic Rate Matching in Heterogeneous Systems
  Advisor: Kevin Skadron
- Shuai Che (*CpE*)
  PhD Proposal Completed in November 2011
  Dissertation Title: Understanding and Optimizing the Performance of Heterogeneous Systems
  Advisor: Kevin Skadron
- Jiawei Huang (*CpE*)
  PhD Defense Completed in April 2012
  Dissertation Title: A Digital System Design Methodology for Efficiency-Quality Tradeoffs Using Imprecise Hardware
  Advisor: John Lach
- Nishant George (*CpE*)
  PhD Proposal Completed in March 2010
  Dissertation Title: Modeling and Mitigating Emerging Transient Faults in Nanoscale Digital Devices
  Advisor: John Lach
- Adam Cabe (*ECE*)
  PhD Defense Completed in September 2010
  Dissertation Title: Power Reduction and Reliability Enhancement Tradeoffs in VLSI Systems
  Advisor: Mircea Stan
- Randy Mann (*ECE*)
  PhD Defense Completed in October 2010
  Dissertation Title: Interactions of Technology and Design in Nano-Scale SRAM
  Advisor: Benton Calhoun
- Hao Huang (*CS*)
  PhD Completed in June 2008
  Dissertation Title: *Storage@desk: A New Mass Storage System with Quality of Service Guarantees for Large Organizations*
  Advisor: Andrew Grimshaw
- Nathanael R. Paul (*CS*)
  PhD Completed in May 2008
  Dissertation Title: *Disk-Level Malware Detection and Response*
  Advisor: David Evans
- Jeremy Sheaffer (*CS*)
  PhD Completed in August 2007
  Dissertation Title: *Physical Challenges in Reliable Graphics Hardware Design*
  Advisor: Kevin Skadron
- Yan Zhang (*ECE*)
  PhD Completed in August 2006
  Dissertation Title: *Temperature-Aware Power Modeling and Optimization in Deep Submicron CMOS*
  Advisor: Mircea Stan
- Tibor Horvath (*CS*)
  PhD Completed in May 2008

Dissertation Title: *Energy Management in Real-Time Multi-Tier Internet Services*
Advisor: Kevin Skadron

- Angshuman Parashar (*Penn State CSE*)
  PhD Completed in May 2007
  Dissertation Title: *Redundancy and Parallelism Tradeoffs for Reliable, High-Performance Architectures*
  Advisor: Anand Sivasubramaniam
- David Tarjan (*CpE*)
  PhD Completed in June 2009
  Dissertation Title: *Efficient Throughput Cores for Asymmetric Manycore Processors*
  Advisor: Kevin Skadron
- Yingmin Li (*CS*)
  PhD Completed in August 2006
  Dissertation Title: *Physically Constrained Architecture for Chip Multiprocessors*
  Advisor: Kevin Skadron

Masters Committees

- Tanima Dey (*CS*
  MCS to be Awarded in May 2011
  Project Title: *Characterizing Multi-Threaded Applications based on Shared-Resource Contention*
  Advisors: Jack Davidson and Mary Lou Soffa
- Prateeksha Satyamoorthy (*Engineering Physics*) - *Committee Chair*
  MS to be Awarded in May 2011
  Thesis Title: *STT-RAM for Shared Memory in GPUs*
  Advisor: Kevin Skadron
- Anurag Nigam (*ECE*)
  MS Completed in May 2010
  Thesis Title: *Self Consistent Parameterized Physical MTJ Compact Model for STT-RAM*
  Advisor: Mircea Stan
- Taniya Siddiqua (*CS*)
  MS Completed in December 2009
  Thesis Title: *Balancing Soft Error Coverage with Lifetime Reliability in Redundantly Multithreaded Processors*
  Advisor: Sudhanva Gurumurthi
- Shuai Che (*CpE*)
  MS Completed in January 2010
  Thesis Title: *Benchmarking GPUs for General Purpose Applications*
  Advisor: Kevin Skadron
- Steven Christopher Jocke (*ECE*)
  MS Completed in May 2009
  Thesis Title: *Design and Application of a Sub-Threshold Core Using a Customized Synthesis Flow*
  Advisor: Benton Calhoun
- Clinton Wills Smullen, IV (*CS*)
  MCS Completed in December 2008
  Project Title: *Revisiting Active Storage for Unstructured Data Processing Applications*
  Advisor: Sudhanva Gurumurthi
- Sriram Sankar
  MS Completed in August 2008
  Thesis Title: *Intra-Disk Parallelism*
  Advisor: Sudhanva Gurumurthi
- Jiayuan Meng (*CS*) - *Committee Chair*
  MCS Completed in August 2007
  Project Title: *Temporal and Spatial Streaming on a General Purpose MIMD Manycore Chip*
  Advisor: Kevin Skadron

- Chris White (*CS*)
  MCS Completed in May 2007
  Project Title: *Managing Data Locality in Hardware with Fractal*
  Advisor: Kevin Skadron
- David Tarjan (*CpE*)
  MS Completed in January 2007
  Thesis Title: *Merging Path, Global, and Local Indexing in Perceptron Branch Prediction*
  Advisor: Kevin Skadron

Undergraduate Students Mentored in Academia

- Daniel Stephen Lee, March 2008
  Thesis Title: *Performance Evaluation of I/O Virtualization in the Xen Architecture*
- Sean Michael Talts (Summer 2007 REU Student)
  Project Topic: *Prototyping and Performance Evaluation of Disk-Level Malware Detection*

Teaching

NOTE: The course and instructor ratings are out of 5.0

Course	Semester	Enrollment	Course Rating	Instructor Rating
CS 654 (Graduate) Computer Architecture	Fall 2005	23	4.10	4.43
CS 851 (Graduate) Advanced Techniques in Computer Architecture and Storage Systems	Spring 2006	8	4.52	4.74
CS 654 (Graduate) Computer Architecture	Fall 2006	29	4.01	4.15
CS 414 (Undergraduate) Operating Systems	Spring 2007	58	4.16	4.18
CS 654 (Graduate) Computer Architecture	Fall 2007	15	4.13	4.36
CS 433 (Undergraduate) Advanced Computer Architecture	Spring 2008	20	3.77	4.15
CS 654 (Graduate) Computer Architecture	Fall 2008	30	4.14	4.26
CS 101E (Undergraduate) Introduction to Computer Science	Spring 2009	88	3.65	3.81
CS 6501 (Graduate) Non-Volatile Memory Systems	Fall 2009	11	4.65	4.76
CS 6354 (Graduate) Computer Architecture	Fall 2010	11	4.07	4.73
CS 1111 (Undergraduate) Introduction to Computer Science	Spring 2011	86	3.99	4.17
CS 6354 (Graduate) Computer Architecture	Fall 2011	20	4.49	4.71
CS 1111 (Undergraduate) Introduction to Computer Science	Spring 2012	89	4.09	4.05

Professional Service

Conference/Workshop Chairmanship

- **Program Co-Chair**, IEEE Workshop on Silicon Errors in Logic - System Effects (**SELSE**), 2016.
- **Program Co-Chair**, IEEE Workshop on Silicon Errors in Logic - System Effects (**SELSE**), 2015.
- **Industry Track Program Chair**, International Symposium on High Performance Computer Architecture (**HPCA**), 2015.
- **Co-Organizer**, Workshop on Integrating Solid-State Memory into the Storage Hierarchy (**WISH**), held in conjunction with ASPLOS 2009.

Conference/Workshop Committees

- **Program Committee**, International Symposium on High Performance Computer Architecture (**HPCA**), 2018.
- **Program Committee**, IEEE International Symposium on On-Line Testing and Robust System Design (**IOLTS**), 2017.
- **External Review Committee**, International Symposium on Microarchitecture (**MICRO**), 2017.
- **Program Committee**, Workshop on Fault Tolerance for HPC at eXtreme Scale (**FTXS**), 2017.
- **Program Committee**, IEEE Workshop on Silicon Errors in Logic - System Effects (**SELSE**), 2017.
- **Program Committee**, International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), 2017.
- **Program Committee**, ACM International Conference on Supercomputing (**ICS**), 2016.
- **Program Committee**, Workshop on Fault Tolerance for HPC at eXtreme Scale (**FTXS**), 2016.
- **External Review Committee**, International Symposium on Computer Architecture (**ISCA**), 2016.
- **Program Committee**, International Symposium on Microarchitecture (**MICRO**), 2015.
- **Program Committee**, International Workshop on Performance Analysis of Workload Optimized Systems (**FASTPATH**), 2015.
- **Program Committee**, International Workshop on Fault Tolerant Systems (**FTS**), 2015.
- **Program Committee**, AMD Asia Technical Conference (**AATC**), 2015.
- **Program Committee**, International Symposium on Computer Architecture (**ISCA**), 2015.
- **Program Committee**, ACM International Conference on Supercomputing (**ICS**), 2015.
- **Technical Advisory Board**, ICCAD Workshop on A Roadmap for EDA Research in the Dark Silicon Era (**EDA4DS**), 2014.
- **Program Committee**, IEEE International On-Line Testing Symposium (**IOLTS**), 2014.
- **Program Committee**, Fast Abstracts Track, International Conference on Dependable Systems and Networks (**DSN**), 2014.
- **Program Committee**, International Workshop on GPU Dependable Computing, 2014.
- **Program Committee**, IEEE Workshop on Silicon Errors in Logic - System Effects (**SELSE**), 2014.
- **Program Committee**, Non-Volatile Memories Workshop (**NVMW**), 2014.
- **Program Committee**, Industry Track, International Symposium on High Performance Computer Architecture (**HPCA**), 2014.
- **Selection Committee**, IEEE Micro Top Picks from Computer Architecture Conferences (**Top Picks**), 2014.
- **Program Committee**, Workshop on Interactions of NVM/FLash with Operating-Systems and Workloads (**INFLOW**), 2013.
- **Program Committee**, Non-Volatile Memories Workshop (**NVMW**), 2013.
- **Program Committee**, IEEE Workshop on Silicon Errors in Logic - System Effects (**SELSE**), 2013.

- **Program Committee**, International Symposium on High Performance Computer Architecture (**HPCA**), 2013.
- **External Review Committee**, International Symposium on Microarchitecture (**MICRO**), 2012.
- **Steering Committee**, Workshop on Energy Consumption and Reliability of Storage Systems (**ERSS**), 2012.
- **Program Committee**, International Green Computing Conference (**IGCC**), 2012.
- **Program Committee**, Non-Volatile Memories Workshop (**NVMW**), 2012.
- **Program Committee**, Workshop on Energy Efficient Design (**WEED**), 2011.
- **Program Committee**, Workshop on Energy Consumption and Reliability of Storage Systems (**ERSS**), 2011.
- **Program Committee**, WOSP/SIPEW International Conference on Performance Engineering (**ICPE**), 2011.
- **Program Committee**, International Symposium on High Performance Computer Architecture (**HPCA**), 2011.
- **Submissions Chair**, International Symposium on High Performance Computer Architecture (**HPCA**), 2011.
- **Program Committee**, IEEE International Symposium on Workload Characterization (**IISWC**), 2010.
- **Program Committee**, Workshop on Energy Efficient Design (**WEED**), 2010.
- **Program Committee**, Workshop on Emerging Storage class memory Technologies (**WEST**), 2010.
- **Program Committee**, USENIX Workshop on Sustainable Information Technology (**SustainIT**), 2010.
- **Program Committee**, USENIX Conference on File and Storage Technologies (**FAST**), 2010.
- **Selection Committee**, IEEE Micro Top Picks from Computer Architecture Conferences (**Top Picks**), 2009.
- **Program Committee**, International Symposium on Computer Architecture (**ISCA**), 2009.
- **Program Committee**, International Symposium on Performance Analysis of Systems and Software (**ISPASS**), 2009.
- **Web Chair**, International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), 2009.
- **Program Committee**, ACM SIGMETRICS Conference on Measurement and Modeling of Computer Systems (**SIGMETRICS**), 2008.
- **Program Committee**, International Symposium on Performance Analysis of Systems and Software (**ISPASS**), 2008.
- **Program Committee**, International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), 2008.
- **Program Committee**, IEEE International Symposium on Workload Characterization (**IISWC**), 2007.
- **Program Committee**, International Conference on Parallel and Distributed Computing and Networks (**PDCN**), 2007.
- **Program Committee**, Reconfigurable and Adaptive Architecture Workshop (**RAAW**), 2006.
- **Program Committee**, Workshop on the Interaction Between Operating System and Computer Architecture (**WIOSCA**), 2006.
- **Program Committee**, International Conference on Parallel Architectures and Compilation Techniques (**PACT**), 2006.
- **Publications Chair**, International Conference on Parallel Architectures and Compilation Techniques (**PACT**), 2006.

Journal Editorship

- Associate Editor, IEEE Computer Architecture Letters, March 2011-March 2014.
- Associate Editor-in-Chief, IEEE Computer Architecture Letters, January 2010-March 2011.

Tutorial Presentations

- Phase Change Memory, with Moinuddin Qureshi (IBM Research) and Bipin Rajendran (IBM Research)

- "System Design with Phase Change Memory - Fundamentals, Opportunities, and Challenges", The Non-Volatile Memories Workshop (NVMW), March 2011. (**140 Registered Attendees**)
- "Phase Change Memory Technology - From Devices to Systems", The International Symposium on Microarchitecture (MICRO), December 2010.
- "Phase Change Memories: A Systems Perspective", The International Symposium on High Performance Computer Architecture (HPCA), January 2010.

Conference Panel Organization

- **Organizer and Moderator**, Technical Panel: *Benchmarking for the Web 2.0 Era*, held at the IEEE International Symposium on Workload Characterization (**IISWC**), Boston, MA September 2007.

Industry Liason for Academic Research (at AMD)

- SRC Liason for "CLASH - Cross-Layer Accelerated Self-Healing: Circadian Rhythms for Resilient Electronic Systems", PI: Mircea Stan (U. Virginia), 2013-2014.

Funding Panels and Site Visit Teams

- National Science Foundation - Engineering Research Center (ERC) site visit review team member in 2014
- National Science Foundation - Numerous
- US Department of Energy - 1 panel

Grant Proposal Peer-Reviewing Activities

- Research Grants Council of Hong Kong, 2012-2017
- National Science Foundation, 2009
- US-Israel Binational Science Foundation, 2009
- Swiss National Science Foundation, 2007
- University of California Energy Institute, 2006

Computer Science Department Service

- Visiting Professor Search Committee, 2012
- Graduate Admissions Committee, 2005, 2007, 2008, 2011
- *Chair*, PhD Qualifying Exam, Computer Architecture Reading List Ad-Hoc Committee, 2007
- Computer Science Graduate Curriculum Committee, 2006, 2009, 2012
- Computer Engineering Graduate Committee, 2009, 2012
- Systems Infrastructure Committee, 2005, 2007

School of Engineering and University Service

- Computer Science Department Chair Search Committee, 2012
- Judge, SEAS Undergraduate Research and Design Symposium (URDS), 2011

Conference and Journal Peer-Reviewing Activities

- *Selected Conferences:* International Symposium on Computer Architecture (ISCA), International Symposium on Microarchitecture (MICRO), International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), International Symposium on High Performance Computer Architecture (HPCA), USENIX Conference on File and Storage Technologies (FAST), International Conference on Dependable Systems and Networks (DSN), International Symposium on Performance Analysis of Systems and Software (ISPASS), ACM SIGPLAN/SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES), International Parallel and Distributed Processing Symposium (IPDPS), International Conference on Supercomputing (ICS)

- *Journals:* IEEE Embedded Systems Letters, ETRI Journal, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, ACM Transactions on Design Automation of Electronic Systems, IEEE Spectrum, IEEE Transactions on Knowledge and Data Engineering, Elsevier Computer Networks, IEEE Transactions on Dependable and Secure Computing, IEEE Computer Architecture Letters, IEEE Transactions on Very Large Scale Integration Systems, ACM/Springer Multimedia Systems Journal, ACM Transactions on Architecture and Code Optimization, ACM Transactions on Storage, IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Computers, GEOINFORMATICA Journal

Miscellaneous Ad Hoc Reviewing Activities

- ACM India Doctoral Dissertation Award, 2016

Textbook Reviewing Activities

- *Computer Systems: An Integrated Approach to Architecture and Operating Systems* by Umakishore Ramachandran (*Georgia Tech*), Addison-Wesley Publishing, 2008.
- *Computer Architecture: A Quantitative Approach* (Fourth Edition) by John Hennessy (*Stanford U.*) and David Patterson (*UC Berkeley*), Morgan Kaufmann Publishers/Elsevier, 2006.
- *Architecture Design for Soft Errors* by Shubhendu Mukherjee (*Intel Corporation*), Morgan Kaufmann Publishers/Elsevier, 2006/2007.

Professional Society Memberships

- IEEE Computer Society (*Senior Member*)
- ACM SIGARCH (*Senior Member*)