

KARTHIK SANKARANARAYANAN

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OBJECTIVE

An industrial research and development position in the areas of computer architecture and its allied disciplines. My current expertise includes power- and thermal-aware modeling and management of microprocessors. I am also interested in exploring other engaging problems in the broad interface between software and hardware.

EDUCATION

Graduate

Department of Computer Science,
University of Virginia, Charlottesville, VA

Ph.D. in Computer Science – expected September 2008

Advisor – Prof. Kevin Skadron, Co-Advisor – Prof. Mircea Stan
Topic: Thermal modeling and management of microprocessors

Master of Computer Science – August 2003, GPA – 3.88 / 4.0

Undergraduate

School of Computer Science and Engineering,
College of Engineering, Guindy, Anna University,
Chennai, India.

B.E. in Computer Science and Engineering

August 1996 – May 2000

GPA – 8.75 / 10.0 (First class with distinction)

WORK EXPERIENCE

- **August 2003 – present** – Graduate Research Assistant, University of Virginia. Advisor – Prof. Kevin Skadron. Area: Thermal modeling and management of microprocessors.
- **Summer 2004** – Intern, Google Inc. Developed a preliminary data collection system to monitor health and activity of machine clusters. Mentor – Dr. Luiz Barroso.
- **July 2001 – August 2003** – Graduate Research Assistant, University of Virginia. Advisor – Prof. Kevin Skadron. Area: Microarchitectural power optimization through profile-based adaptation for cache decay.
- **Summer 2002** – Research intern, Microsoft Research – Performance Monitoring and Analysis group, Programmer Productivity Research Center. Worked on characterizing memory performance of applications. Mentor – Dr. Scott McFarling. Manager – Dr. Ben Zorn.
- **August 2000 – May 2001** – Graduate Teaching Assistant, University of Virginia. TA for the OS course (CS 414) for two semesters.

RESEARCH

As a member of the LAVA (Laboratory of Architecture at Virginia) lab, I work under the primary guidance of Prof. Kevin Skadron in the areas of temperature and power-aware processor microarchitecture. My co-advisor is Prof. Mircea Stan who heads the HPLP (High Performance Low Power VLSI) lab. Our groups have developed 'HotSpot' (<http://lava.cs.virginia.edu/HotSpot/>) - an accurate and computationally efficient thermal simulator to model processor temperature at the architecture level. It also comprises of 'HotFloorplan', a thermally-aware floorplanner that can be used for microarchitectural studies. HotSpot has been downloaded by more than one thousand users and is widely used in the computer architecture community.

My Ph.D. dissertation involves work to address the temperature challenge from the perspective of the architecture of the microprocessor. It proposes both the infrastructure to model the problem (HotSpot and HotFloorplan) and several mechanisms that form part of the solution. It describes the construction and use of HotSpot software to guide the design and evaluation of various static and dynamic thermal management techniques. Processor temperature is not only a function of the power density but also the placement and adjacency of hot and cold functional blocks. Hence, using HotFloorplan, the dissertation also evaluates a variety of single core and multi-core placement choices. Through an analytical framework, it also addresses the question of the spatial (size) granularity at which thermal modeling and management are important. If regions of very high power density are small enough, they do not cause hot spots. The granularity study attempts to quantify this relationship. Finally, for real-time applications, it also investigates a scheme to reconcile the reactive nature of run-time thermal management with the scheduling constraint of meeting the deadlines.

For my Masters' project, I worked on a profile-based adaptation technique for 'cache decay'. Cache decay is a leakage reduction mechanism that saves static power by shutting off dead cache lines. Unused lines are identified by waiting for a particular period of time called the decay interval. Any line that remains untouched during that period is considered dead and is shut down. My Masters' work explored the adaptation of this decay interval through profiling. The main finding was that almost all the parameters that determine the optimal value of the decay interval could be estimated through static profiling. The profile-based adaptation technique performed better than previously proposed online adaptation schemes.

SELECTED REFEREED PUBLICATIONS

Journals

- [1] W. Huang, K. Sankaranarayanan, R. J. Ribando, M. R. Stan, and K. Skadron. "Accurate, Pre-RTL Temperature-Aware Processor Design Using a Parameterized, Geometric Thermal Model" To appear in the IEEE Transactions on Computers
- [2] W. Huang, S. Ghosh, S. Velusamy, K. Sankaranarayanan, K. Skadron and M. R. Stan. "HotSpot: A Compact Thermal Modeling Method for CMOS VLSI Systems." IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 14(5):501-513, May 2006
- [3] K. Sankaranarayanan, S. Velusamy, M.R. Stan, and K. Skadron. "A Case for Thermal-Aware Floorplanning at the Microarchitectural Level." The Journal of Instruction-Level Parallelism, vol. 7, Oct. 2005, <http://www.jilp.org/vol7/>
- [4] K. Sankaranarayanan and K. Skadron. "Profile-Based Adaptation for Cache Decay". ACM Transactions on Architecture and Code Optimization, 1(3):305-322, Sep. 2004
- [5] K. Skadron, M.R. Stan, K. Sankaranarayanan, W. Huang, S. Velusamy and D. Tarjan. "Temperature-Aware Microarchitecture: Modeling and Implementation." ACM Transactions on Architecture and Code Optimization, 1(1):94-125, Mar. 2004
- [6] K. Skadron, M.R. Stan, W. Huang, S. Velusamy, K. Sankaranarayanan, and D. Tarjan. "Temperature-Aware Computer Systems: Opportunities and Challenges." IEEE Micro, 23(6):52-61, Nov-Dec. 2003 (Special issue on "Top Picks from Microarchitecture Conferences" for 2003)

Conferences and Workshops

- [1] W. Huang, M. R. Stan, K. Sankaranarayanan, R. J. Ribando, and K. Skadron. "Many-Core Design from a Thermal Perspective." In Proceedings of the 45th ACM/IEEE Conference on Design Automation (DAC), June 2008, to appear
- [2] W. Huang, K. Sankaranarayanan, R. J. Ribando, M. R. Stan, and K. Skadron. "An Improved Block-Based Thermal Model in HotSpot-4.0 with Granularity Considerations." In Proceedings of the Workshop on Duplicating, Deconstructing, and Debunking, in conjunction with the 34th International Symposium on Computer Architecture (ISCA), June 2007
- [3] W. Huang, M. R. Stan, K. Skadron, K. Sankaranarayanan, S. Ghosh and S. Velusamy. "Compact Thermal Modeling for Temperature-Aware Design." In Proceedings of the 41st ACM/IEEE Design Automation Conference (DAC), pp. 878-883, June 2004
- [4] Y. Li, D. Parikh, Y. Zhang, K. Sankaranarayanan, M. R. Stan, and K. Skadron. "State-Preserving vs. Non-State-Preserving Leakage Control in Caches." In Proceedings of the 2004 Design, Automation and Test in Europe (DATE) Conference, pp. 22-27, Feb. 2004
- [5] K. Skadron, M. R. Stan, W. Huang, S. Velusamy, K. Sankaranarayanan, and D. Tarjan. "Temperature-Aware Microarchitecture." In Proceedings of the 30th International Symposium on Computer Architecture (ISCA), pp. 2-13, June 2003 (Best student paper!)
- [6] S. Velusamy, K. Sankaranarayanan, D. Parikh, T. Abdelzaher, and K. Skadron. "Adaptive Cache Decay using Formal Feedback Control." In Proceedings of the Workshop on Memory Performance Issues (WMPI), held in conjunction with ISCA-29, May 2002
- [7] R. Parthasarathi, E. Raman, K. Sankaranarayanan and L. N. Chakrapani, "A Reconfigurable Co-Processor for Variable Long Precision Arithmetic Using Indian Algorithms", In Proceedings of the IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), Apr. 2001

TEACHING EXPERIENCE

University of Virginia

- Guest lectures on cache organization for the graduate Computer Architecture class (CS 654)
- Teaching assistant for the undergraduate Operating Systems class (CS 414) during Fall 2000 and Spring 2001 semesters

Anna University

- Summer and winter classes on traditional Indian sciences as part of the InSIGHT seminar for high school children
- Evening classes on C programming for first year students conducted by the Computer Society of Anna University

AWARDS AND HONORS

Best student paper at ISCA 2003

PROFESSIONAL ACTIVITIES

- **Memberships:** Student member of the ACM, SIGARCH and SIGMICRO
- **Paper reviews:** Journals – TVLSI, TCAD, JOLPE, MEJ; Conferences – ISCA, ASPLOS, MICRO

RELEVANT GRADUATE COURSEWORK

Computer Architecture, Advanced Computer Architecture, VLSI, Software Dynamic Translation, Stochastic Systems, Digital Control Systems (audited), Compilers (audited), Algorithms, Physically-Aware Design, SOC Design (audited)

SOFTWARE SKILLS

- **Assembly Languages** – 80x86, SPARC, MIPS
- **High Level Languages** – C, C++, Perl, Java
- **Platforms** – UNIX (Solaris, FreeBSD, Linux), Windows (9x, NT, 2000, XP, Vista), DOS
- **Hardware Design** – VHDL, Xilinx Foundation Series tools, Cadence IC design tools
- **Compiler Tools** – Vulcan (binary rewriter), Strata (dynamic translator), GNU programming tools
- **Architecture Simulators** – SimpleScalar, Wattch, Turandot, PowerTimer
- **Thermal Modeling** – ANSYS

PERSONAL INFORMATION

- Visa Status – F1
- Country of Citizenship – India

REFERENCES

Available upon request