CS3330 Exam 2 – Spring 2015

Name: _____

Directions: Put the letter of your selection or the short answer requested in the box. **Write clearly**: if we are unsure what you wrote you will get a zero on that problem.

Test proctors will *not* provide clarification during the exam. If you find something **ambiguous** or unclear, explain that clearly on your exam and add a * to the top right corner of your answer box so we know to look for your note when grading.

If you do not sign the pledge on the last page you will get a zero on the entire exam.

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Question 1: In the FDEMW five-stage pipeline we analyzed in class, if we want to stall writeback which many pipeline register(s) should be given the "bubble" signal? Select all that apply

A the register before fetch
B the register before decode
C the register before memory
D the register before writeback
E the register before execute
F none of the above

Answer: *F*

Question 2: If we cut power for one millisecond, which of the following is true?

A SRAM would keep its data, DRAM would keep its data
B SRAM would keep its data, DRAM would lose its data
C SRAM would lose its data, DRAM would lose its data
D SRAM would lose its data, DRAM would keep its data

Answer: *D*

Question 3: To implement data forwarding, we had to check if each source of one instruction was either destination of any earlier instruction still in the pipeline somewhere. Without data forwarding, which of the following is true?

A the check for stalling decode doesn't involve sources and destinations
B we need to compare sources and destinations to decide if we stall decode, but it is a much simpler check
C we need the same check to decide if we stall decode
D the above answers are misleading: removing data forwarding doesn't result in stalling decode

Answer: *C*

Question 4: If you organize current storage technologies from fastest to slowest, you have also organized them from most expensive to least expensive. This is because

A slow-and-expensive technologies don't survive in the market so they don't make the list
B it's cause-and-effect: running quickly consumes money
C it's cause-and-effect: spending money makes things faster
D it's just a coincidence; new technologies could change that

Answer: *A*

Question 5: In the FDEMW five-stage pipeline we analyzed in class, if we want to stall memory how many pipeline registers should be given the "stall" signal?

A 4
B 5
C 0
D 2
E 3
F 1

Answer: *A*

Question 6: In the FDEMW five-stage pipeline we analyzed in class, if we want to stall decode how many pipeline registers should be given the "normal operation" signal?

A 3
B 0
C 4
D 5
E 2
F 1

Answer: *E*

Question 7: Capacity misses are typically discussed in connection with

A direct-mapped caches
B fully-associative caches
C set-associative caches
D all of the above
E none of the above

Answer: *B*

Question 8: In the simulators we worked with the register file had two write ports, dstE/wvalE and dstM/wvalM. However, only the `popl` operations used them both. Which two registers are written by `popl %eax`? Write two letters in the box (e.g., if you think it is the first two options, write AB)

A ebp
B esp
C edx
D ebx
E eax
F ecx
G esi
H edi

Answer: *E*

Question 9: In the FDEMW five-stage pipeline we analyzed in class, if we want to bubble decode how many pipeline registers should be given the "normal operation" signal?

A 2
B 1
C 0
D 3
E 4
F 5

Answer: *E*

Question 10:
Consider the 10-bit address $ABCDEFGHIJ$, where each letter represents one bit. With 8-byte blocks, 4 lines per set, and 16 sets, what is the tag? Write your answer in the box; e.g., if you think the answer is the first two bits write AB.

Answer: *ABC*

Question 11: Suppose one stage of a pipeline depends on data forwarded from another, later stage. This describes a

A dependency
B hazard
C a hazard for some pipelines (depending on how many stages there are and/or how many stages are in between the two)
D a dependency for some pipelines (depending on how many stages there are and/or how many stages are in between the two)

Answer: *B*

Question 12: Conflict misses are typically discussed in connection with

A set-associative caches
B fully-associative caches
C direct-mapped caches
D all of the above
E none of the above

Answer: *C*

Question 13: Set-associative cache X breaks a 32-bit address into a 20-bit tag and a 4-bit block offset. How many sets are there in X?

A it depends on how many lines there are per set
B 8
C $2^8 = 256$
D $log_2(8) = 3$
E none of the above

Answer: *C*

Question 14: If we cut power for one minute, which of the following is true?

A SRAM would lose its data, DRAM would lose its data
B SRAM would lose its data, DRAM would keep its data
C SRAM would keep its data, DRAM would keep its data
D SRAM would keep its data, DRAM would lose its data

Answer: *A*

Question 15: Dirty bits are associated with (pick the best answer):

A write-through caches
B set-associative caches
C write-back caches
D direct-mapped caches
E fully-associative caches
F all of the above have dirty bits
G none of the above have dirty bits

Answer: *C*

Question 16: In the simulators we worked with the register file had two write ports, dstE/wvalE and dstM/wvalM. However, only the `popl` operations used them both. Consider a design where we have only one write port (i.e., the register file can only write one value per cycle) and we implement `popl` to write one value in writeback one cycle, then to stay in writeback and write the other value the next cycle. This design

A Can't work
B Can work, but will stall sometimes, depending on what instruction precedes `popl`
C Can work, but will stall sometimes, depending on what instruction follows `popl`
D Can work, but will always stall for every `popl` instruction

Answer: *D*

Question 17: When reading from a direct-mapped cache, which of the following will result in a cache miss? Select all that apply by writing one or more letters in the box. Note: some answers are nonsensical, misusing terminology; do not select those answers.

A address's tag does not match cache line's tag
B address's valid bit does not match cache line's valid bit
C address's dirty bit does not match cache line's dirty bit
D the cache line's tag is set
E the cache line's dirty bit is set
F the cache line's valid bit is set
G none of the above apply

Answer: *A*

Question 18: Fully-associative cache X has 8-byte lines with 32 lines in the cache. If addresses are 12 bits long, how long is the tag?

A 4
B it depends on how many lines there are per set
C $2^4 = 16$
D $log_2(4) = 2$
E none of the above

Answer: *E*

Question 19: Magnetic disk seek time is made up of time needed to get to the right track and time needed to get to the right sector. Which of these involves physical motion?

A both
B finding the sector
C neither
D finding the track

Answer: *A*

Question 20: In a set-associative cache, which of the following does *not* need to be a power of two?

A lines per set
B bytes per block
C number of sets
D all of the above must be powers of two

Answer: *A*

Question 21: Supposed a set-associative cache has a fixed total capacity of 128KB. To prioritize the performance of code that exhibits high temporal locality but low spatial locality, the cache should (pick the most correct answer):

A have small sets
B have large sets
C have small blocks
D have large blocks
E none of the above prioritizes temporal over spatial locality

Answer: *C*

Question 22: Addresses A, B, and C all have the same set index; A and B have the same tag but C's tag is different; B and C have the same block offset but A's block offset is different.

Starting from a cold direct-mapped cache, how many hits are there when executing the following five reads in order: A, B, C, A, B?

A 0
B 5
C 1
D 3
E 2
F 4

Answer: *E*

Question 23: In the simulators we worked with the register file had two write ports, dstE/wvalE and dstM/wvalM. However, only the `popl` operations used them both. Consider a design where we have only one write port (i.e., the register file can only write one value per cycle) and we implement `popl` to write use that write port twice, once during its memory phase and once during its writeback phase. This design

A Can't work
B Can work, but will stall sometimes, depending on what instruction follows `popl`
C Can work, but will always stall for every `popl` instruction
D Can work, but will stall sometimes, depending on what instruction precedes `popl`

Answer: *D*

Question 24: Cold misses are typically discussed in connection with

A fully-associative caches
B set-associative caches
C direct-mapped caches
D all of the above
E none of the above

Answer: *D*

Question 25: Given two caches A and B in a cache hierarchy, where A is closer to the CPU and B is closer to main memory. For *every* cache hierarchy

A size(A) > size(B) and speed(A) > speed(B)
B size(A) < size(B) and speed(A) < speed(B)
C size(A) > size(B) and speed(A) < speed(B)
D size(A) < size(B) and speed(A) > speed(B)
E None of the above are true of every cache hierarchy

Answer: *D*

Pledge:

On my honor as a student, I have neither given nor received aid on this exam.

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