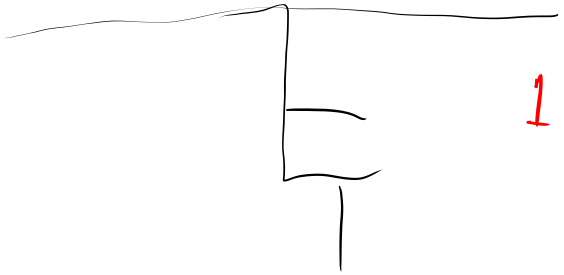
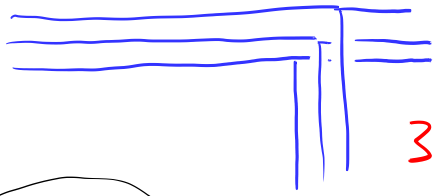
Wires

Connects electrically



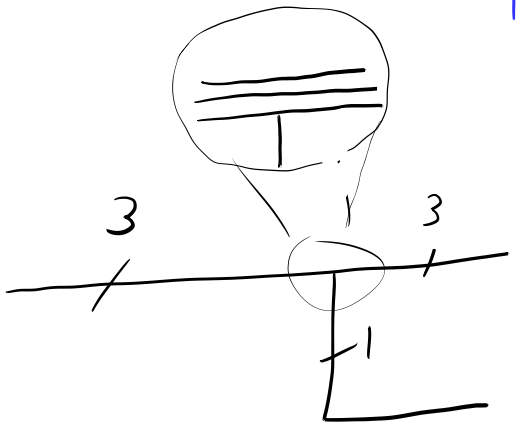
1 bit

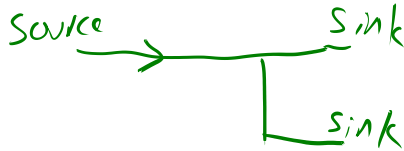
Multi-bit



3-bit wire

wire with width 3





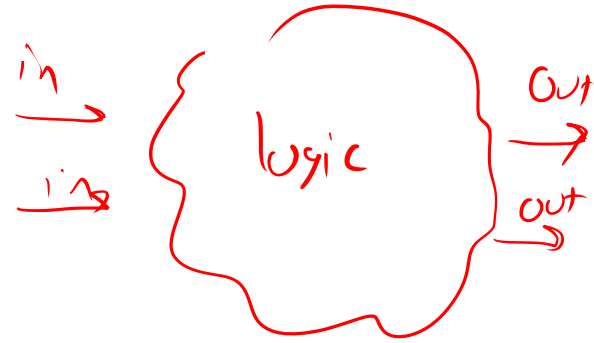
1 signal source

not 0: capacitance

not 2: short circuit

any # of sinks

Gates and "Logic"



transistor
- voltage-triggered switch
- build gates (4-6 trans) and or not

acyclic network of gates "logic"
- can compute any finite function

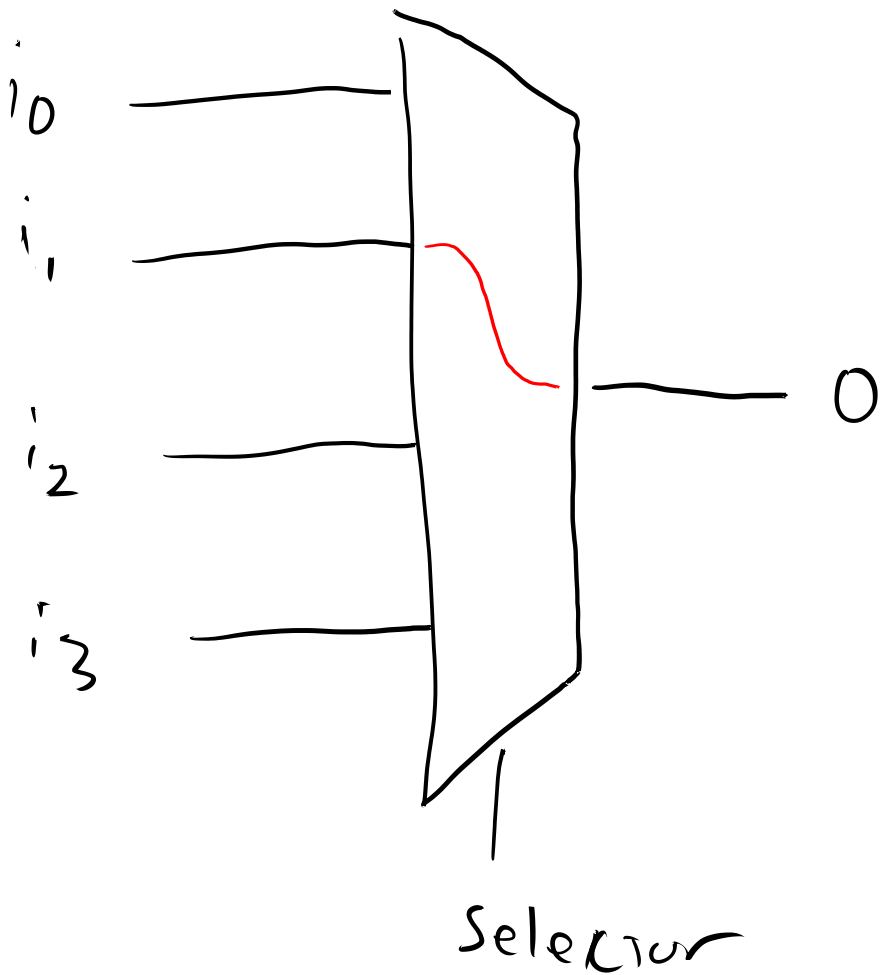
efficient: operate in code

&
|
+
*

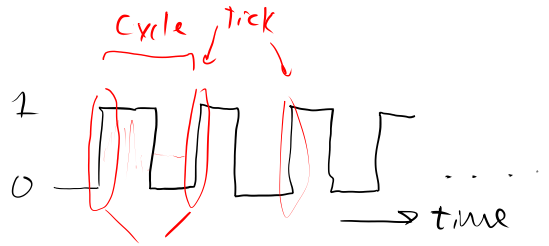
Mutiplexer
Mux

$O = b ? i_1 : i_0$

$O = inputs[selector]$



Registers

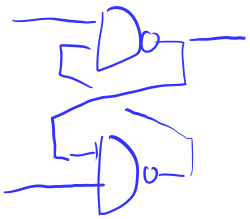


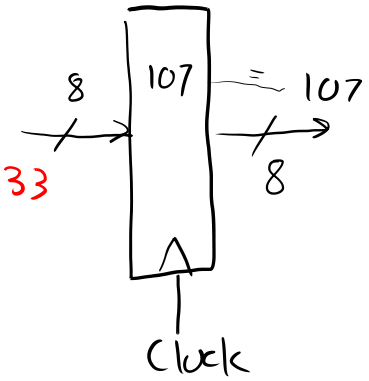
registers change stored value to match input

Cyclic gates

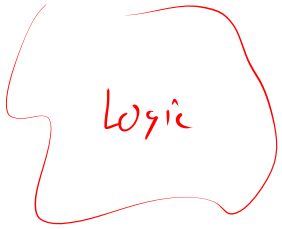
↳ store things

State

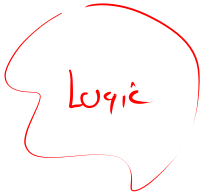




State at time = 0



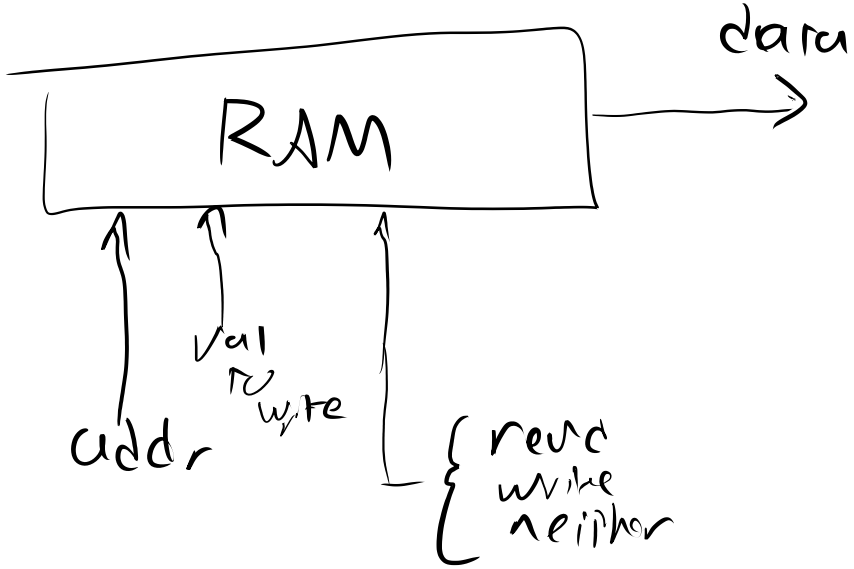
State at time 1



State at time 2

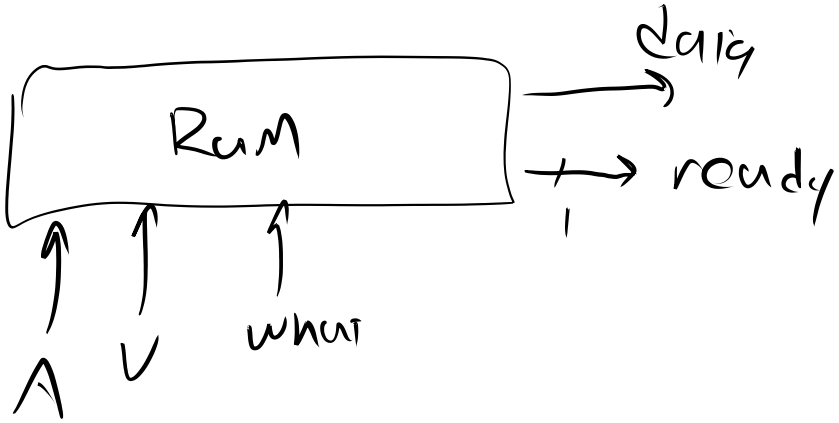
Memory

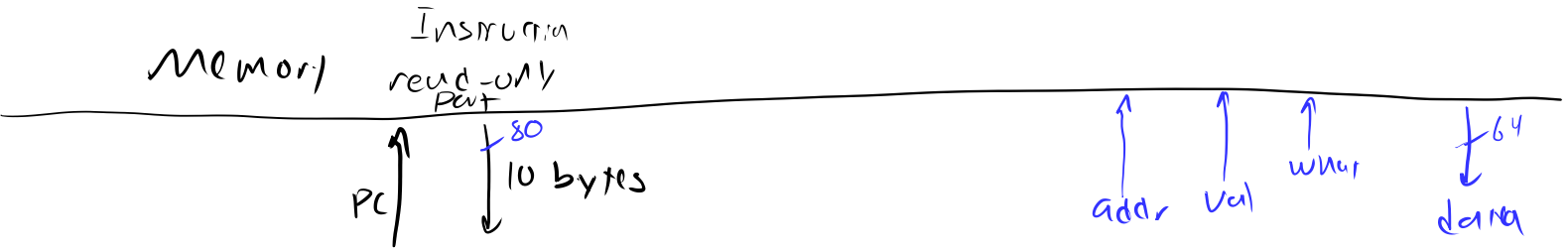
Simple

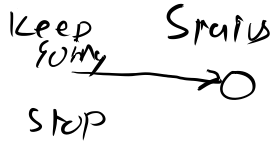


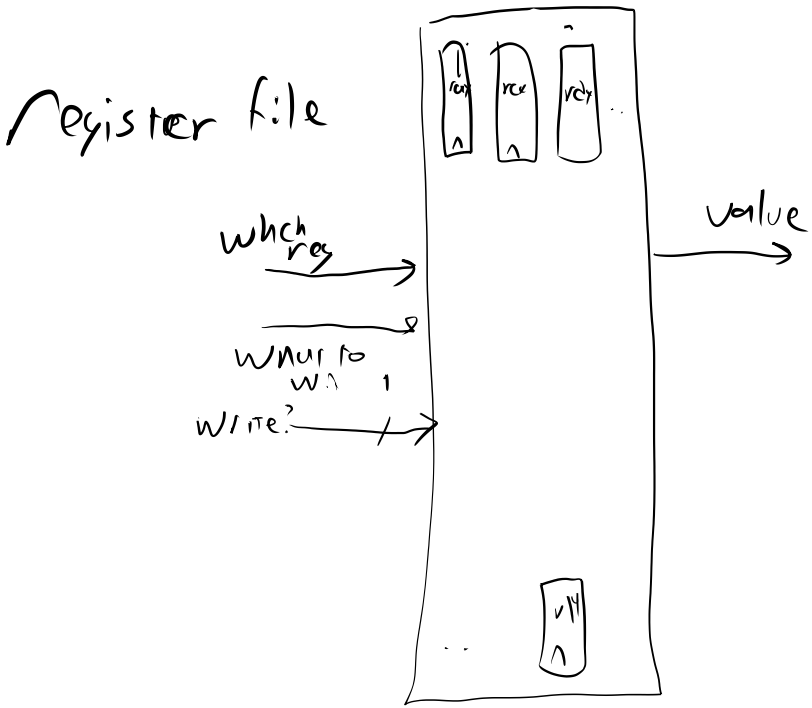
each cycle : 1 thing

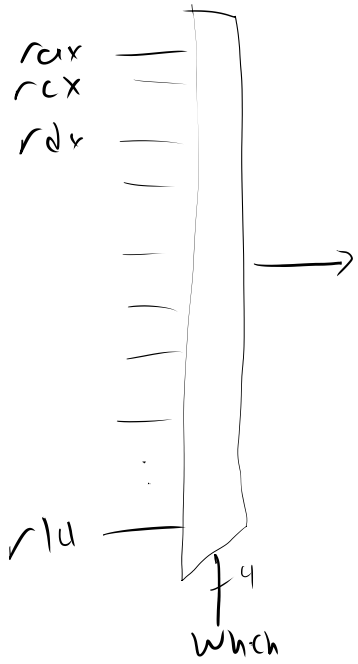
Complex




Memory
Instruction
read-only
port
PC
80
10 bytes
addr
val
wnum
64
data


keep
going
Status
stop


register file
rax
rcx
rdx
rsp
which reg
value
wnum to
write?
1


rax
rcx
rdx
r14
4
which