	Reg	vs	Mem
HW:	↑ fast		slow
	few		lots of
SW:	names		addresses

RAM
↳ w/ 16 addresses

Stage ≈ clock cycle / Yes - PIPE
\ No - SEQ

time

Gate delay $\sim 10_{ps}$


1
2
2
2
2 (bits) - 1
70ps

F - mem - 1 ns

D ~ 40 ps
80 ps

F 1270 ps
40 ps
40 ps

M 40 ps
mem - 1 ns

W 40 ps

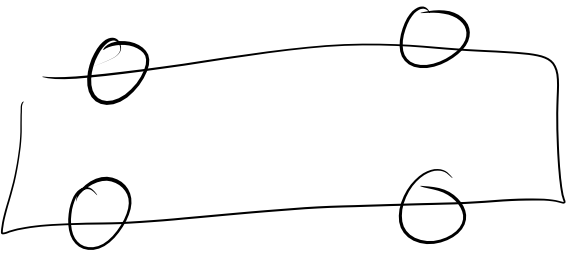
3.67 ns

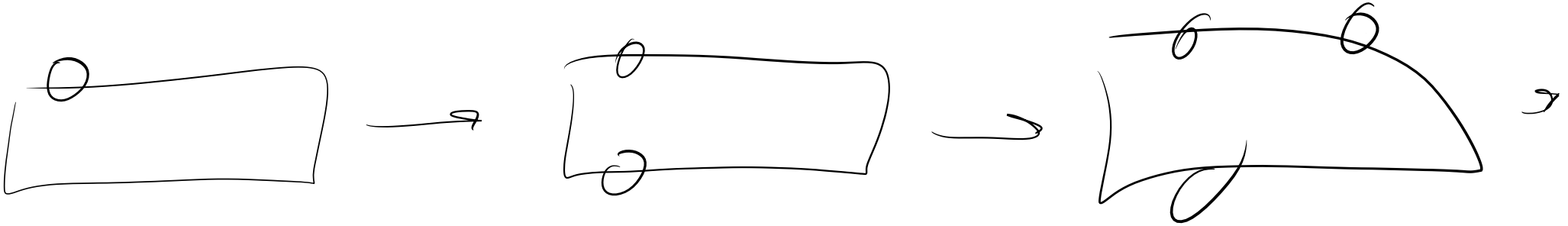
read 4 ns ~ 250 MHz

Pipelining

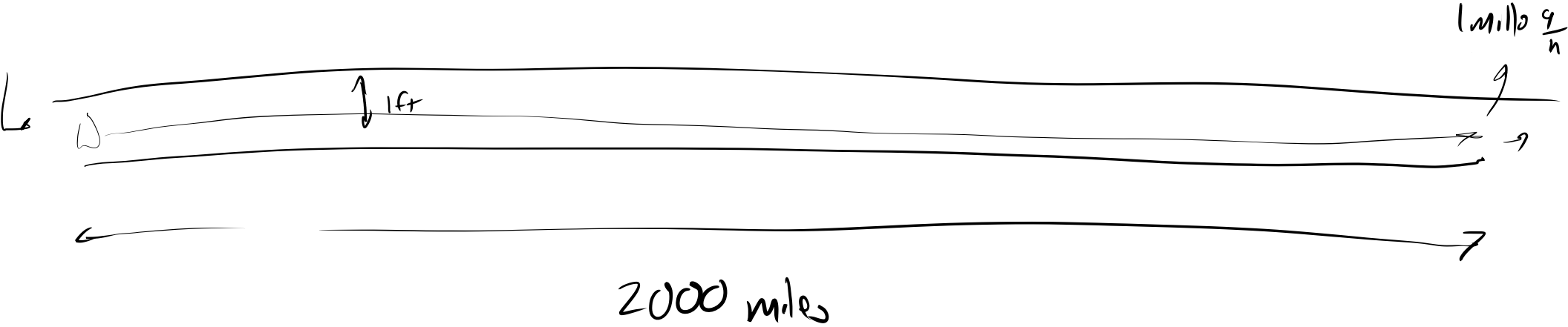
latency - $\frac{\text{time}}{\text{task}}$ 1 task

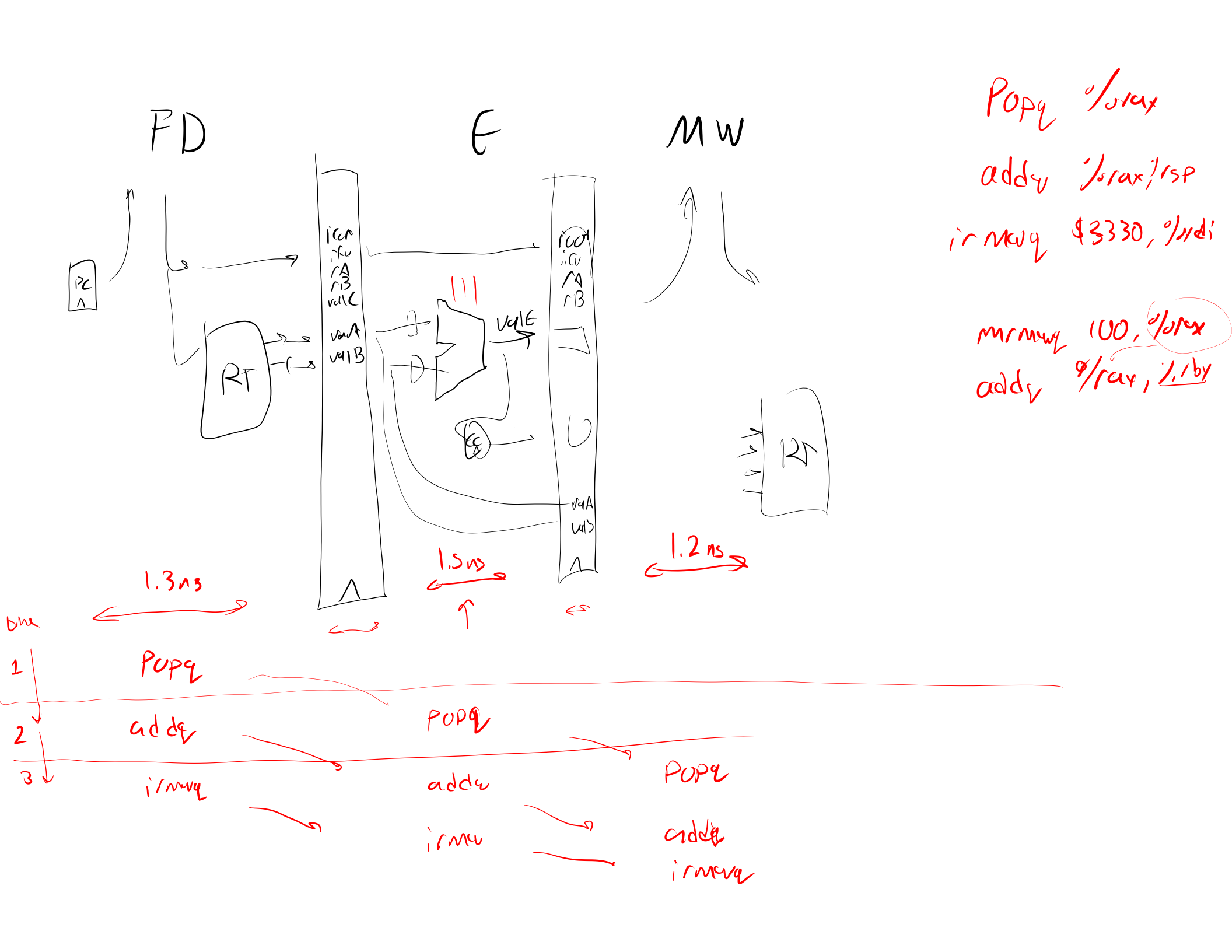
throughput - $\frac{\text{tasks}}{\text{time}}$ many tasks





Pipeline





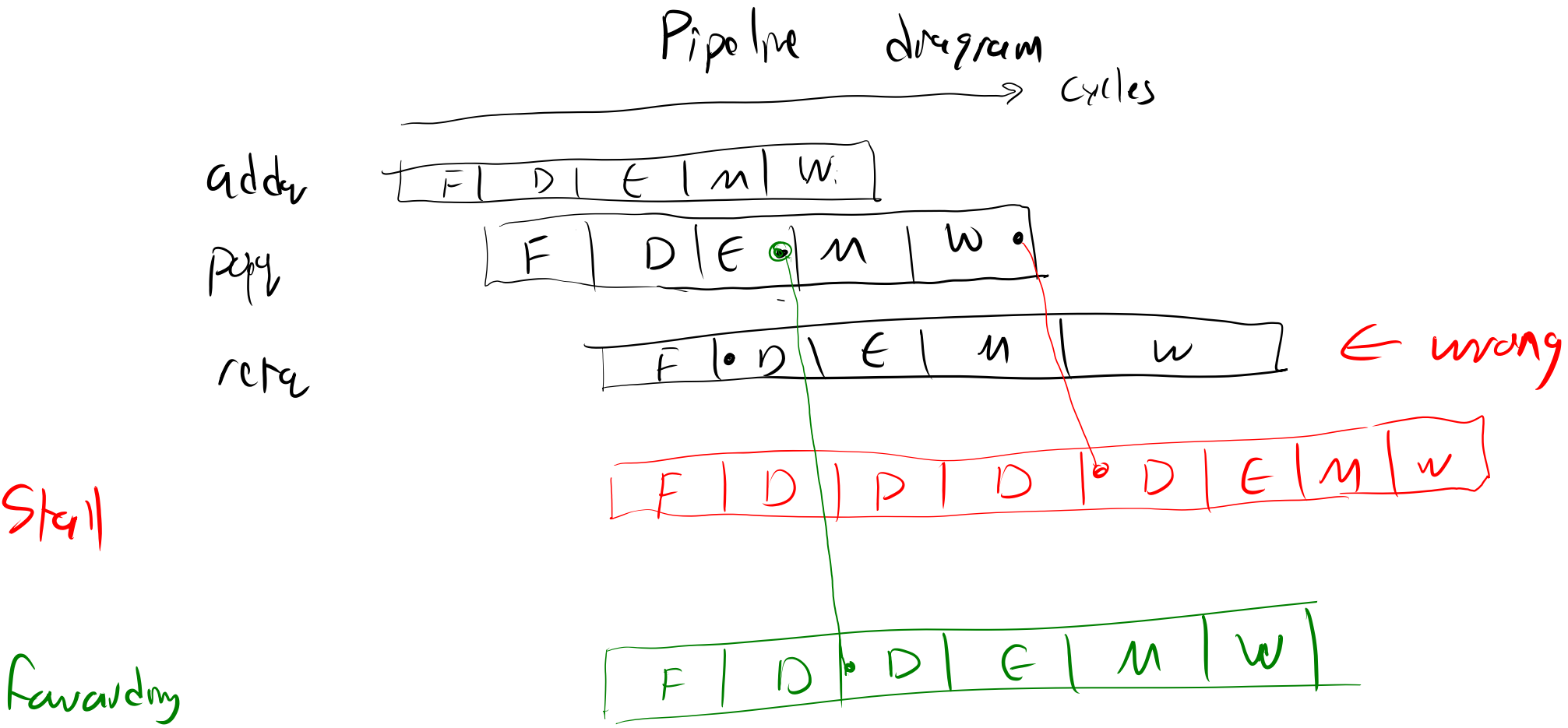
popq %rax

addq %rax, %rsp

irmovq $3330, %rdi

mrmovq 100, %rax

addq %rax, 1,1by


Pipeline diagram
cycles
add
pop
ret
F D E M W
F D E M W
F D E M W
← wrong
Stall
F D D D D E M W
forwarding
F D D E M W