



DRAM

volatile

slower

\$

fast

\$

SRAM

faster

\$\$\$

RAM

random

access

memory

Flash

storage

fast

\$\$

Mag. disk

slower

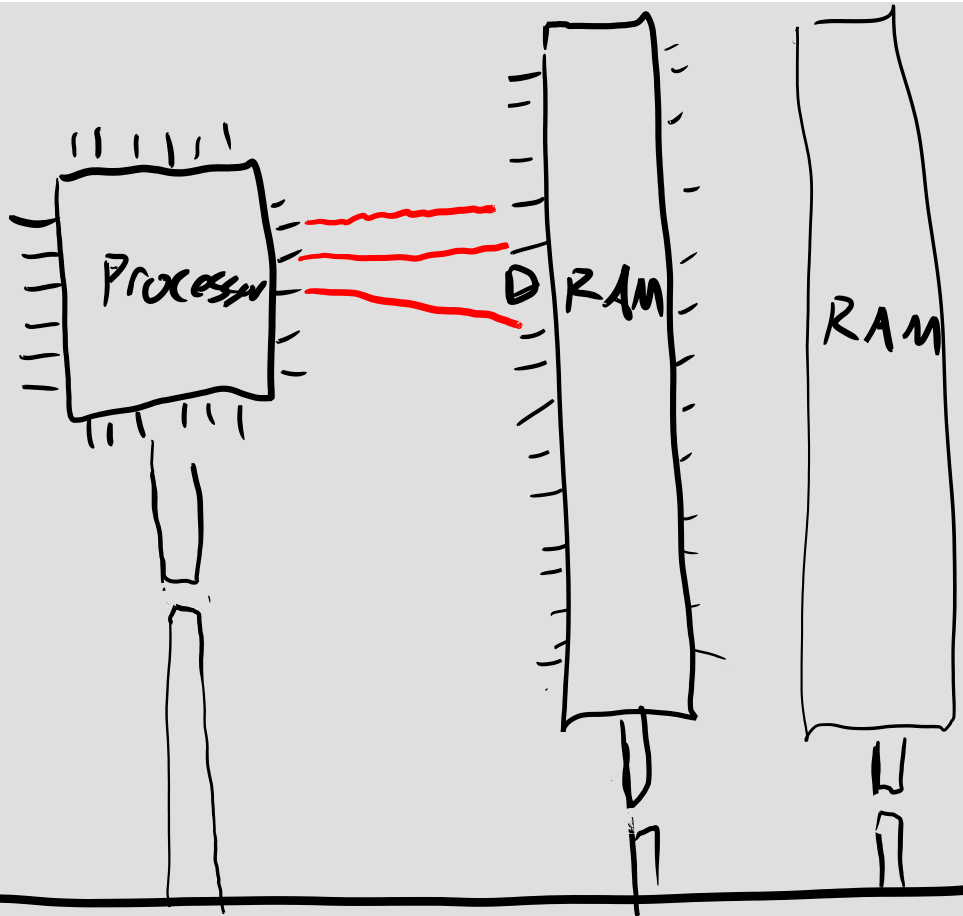
\$

files

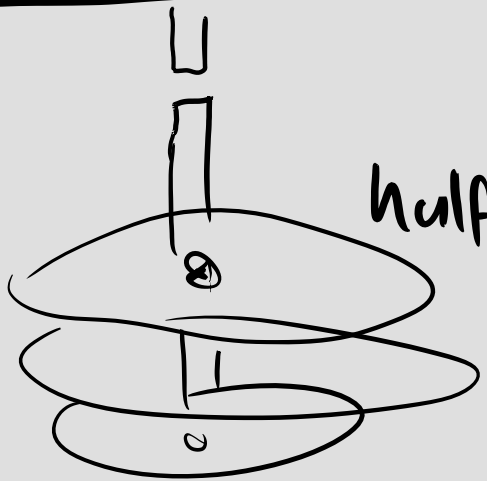
ROM

read-only-memory

Mem\_wire = . . . .




Read chip 1  
req  
from indx  
seq # bytes



Bus  
wire  
half-duplex

$$R_{eq}(3) = R_{eq}(s) \cdot T2$$

Mem [  ]

166B

$2^{34}$

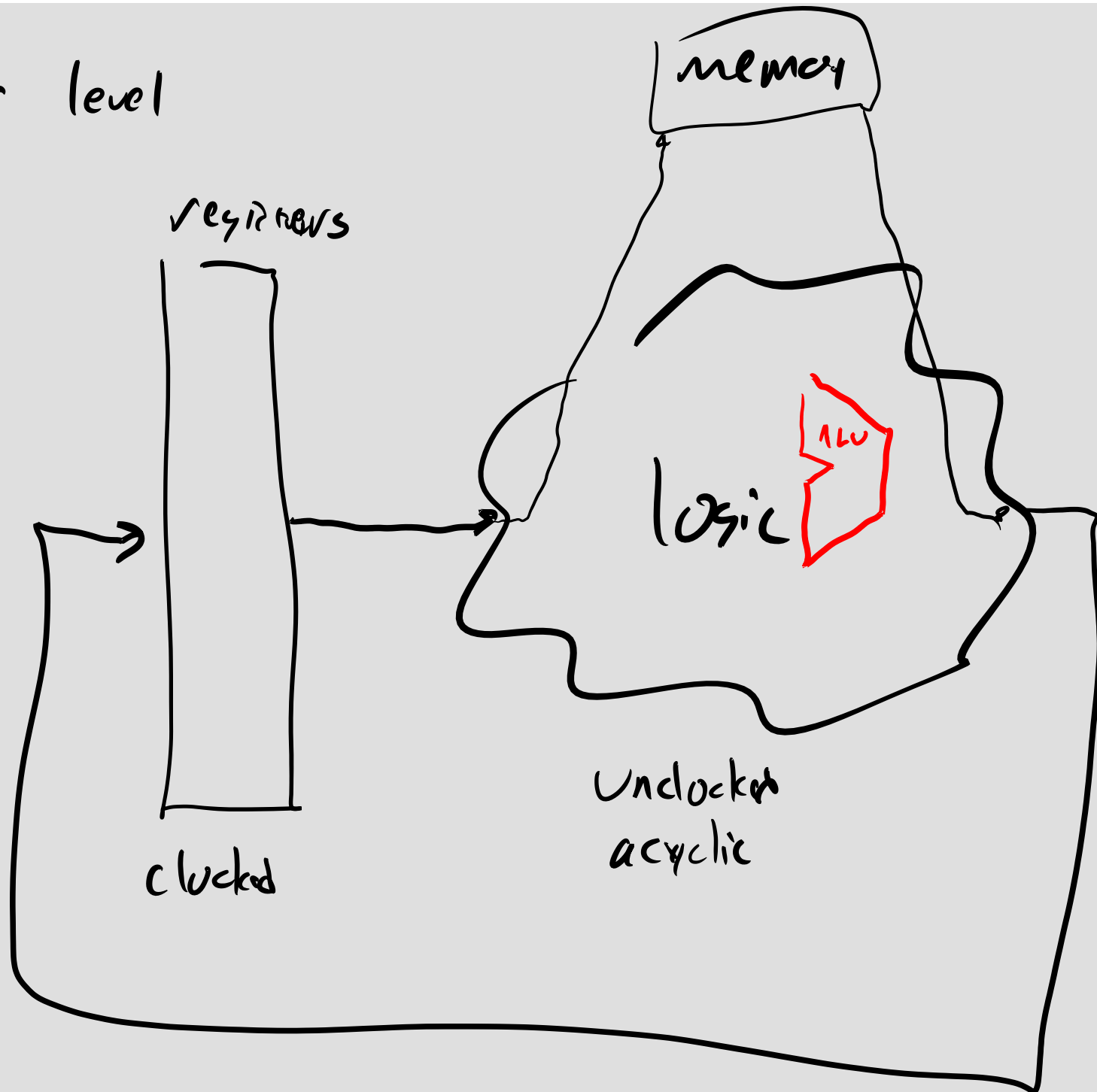
Moore

18 menish

CPU

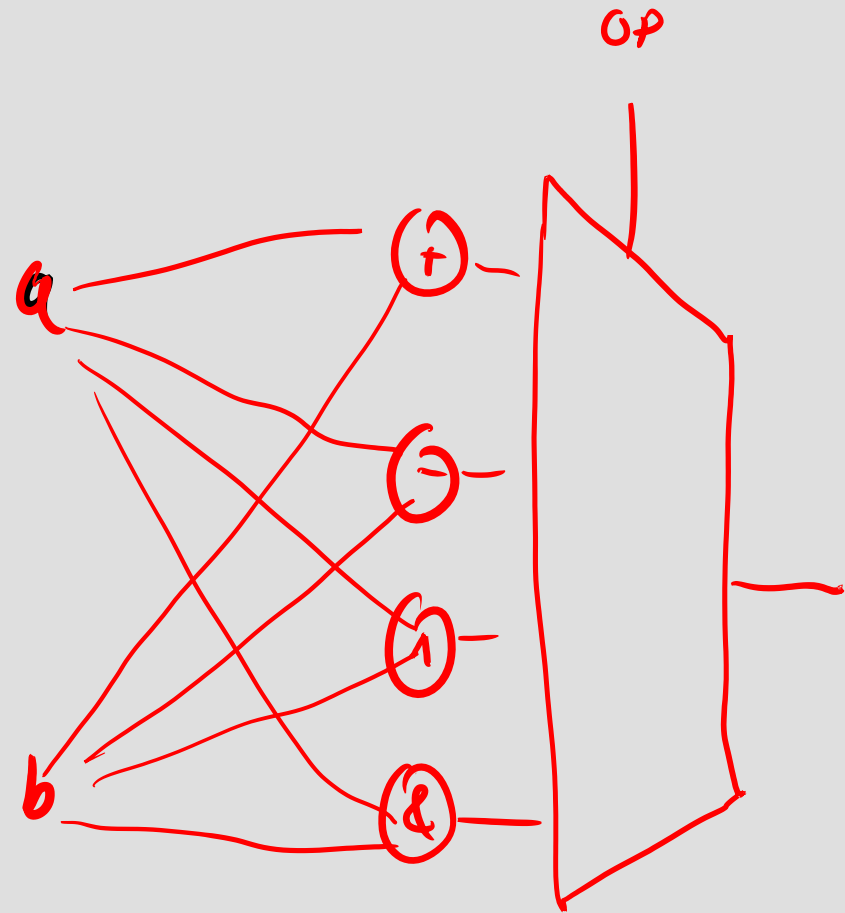
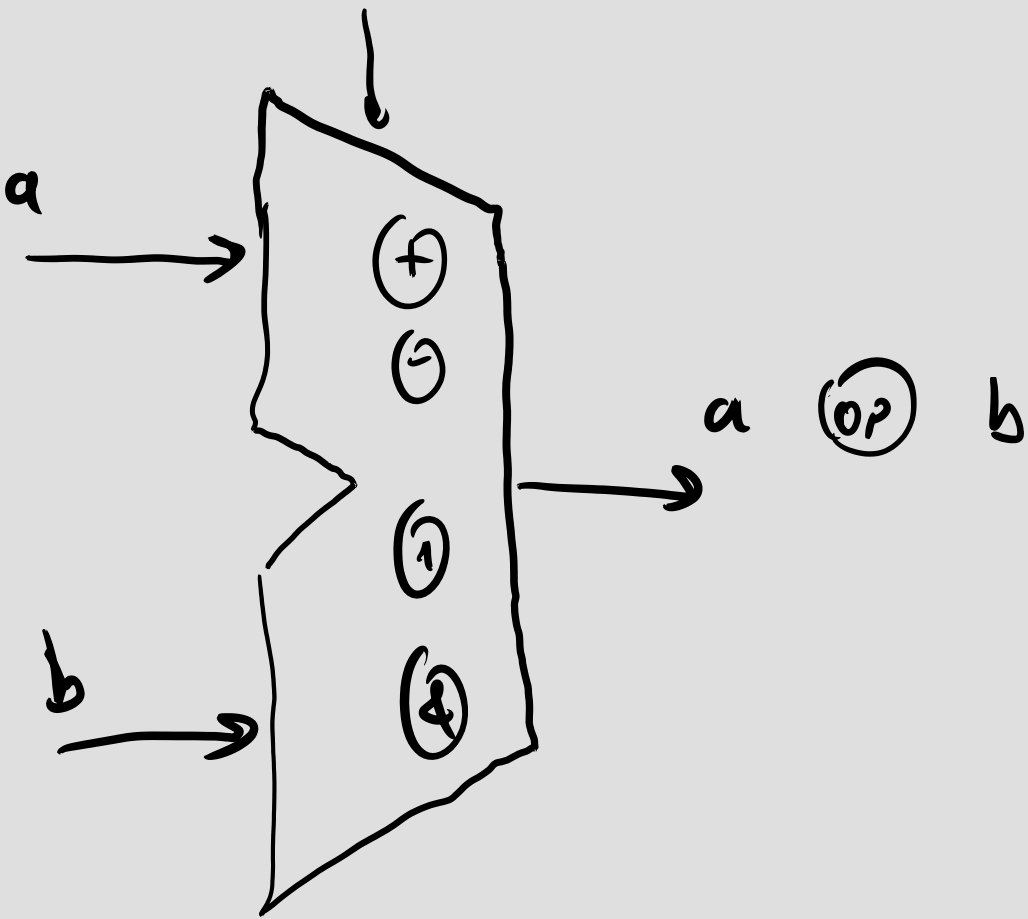
2x fast

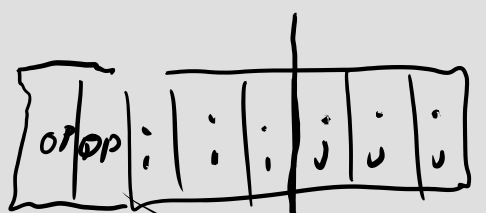
# Register - Transfer level



# ALU

OP Arithmetic-logic Unit





$R[i] = R[j]$

