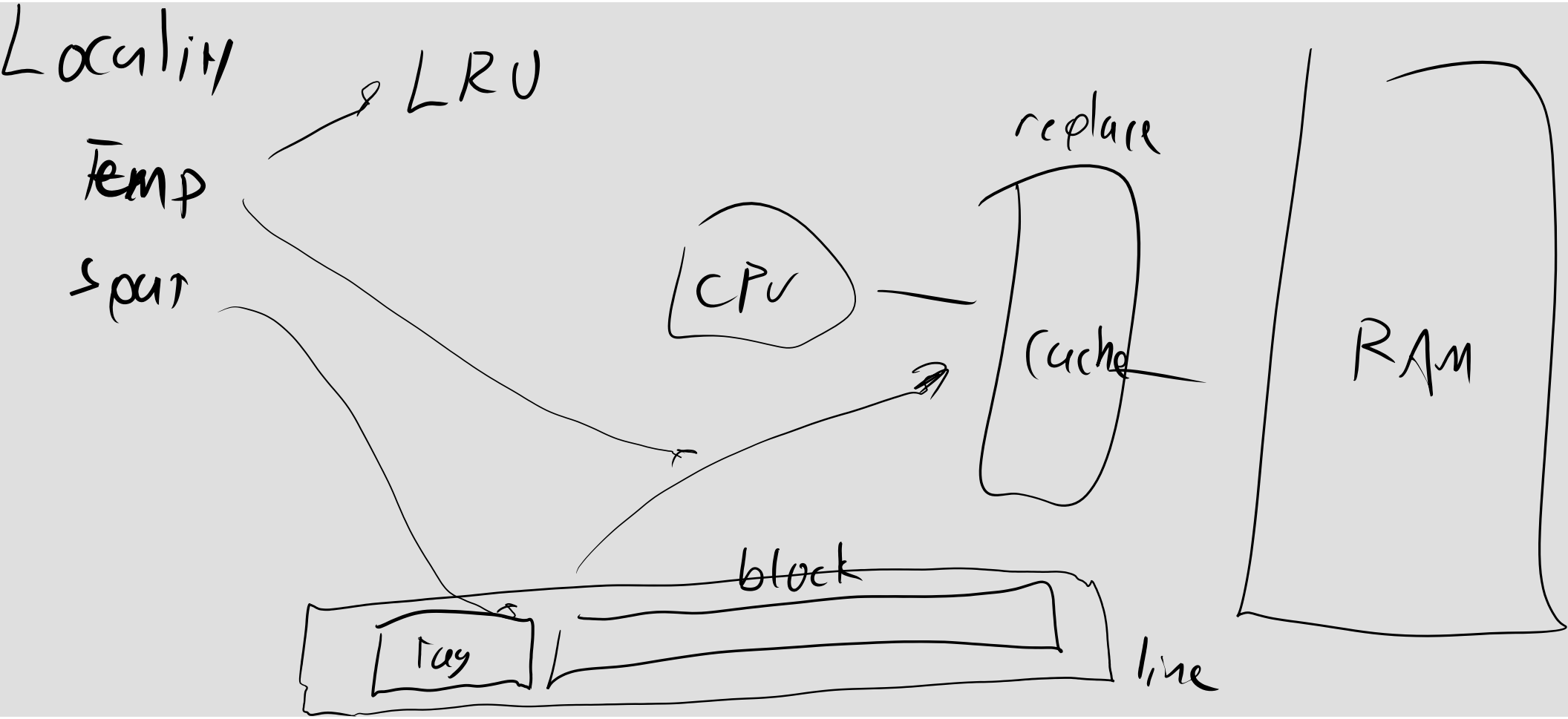
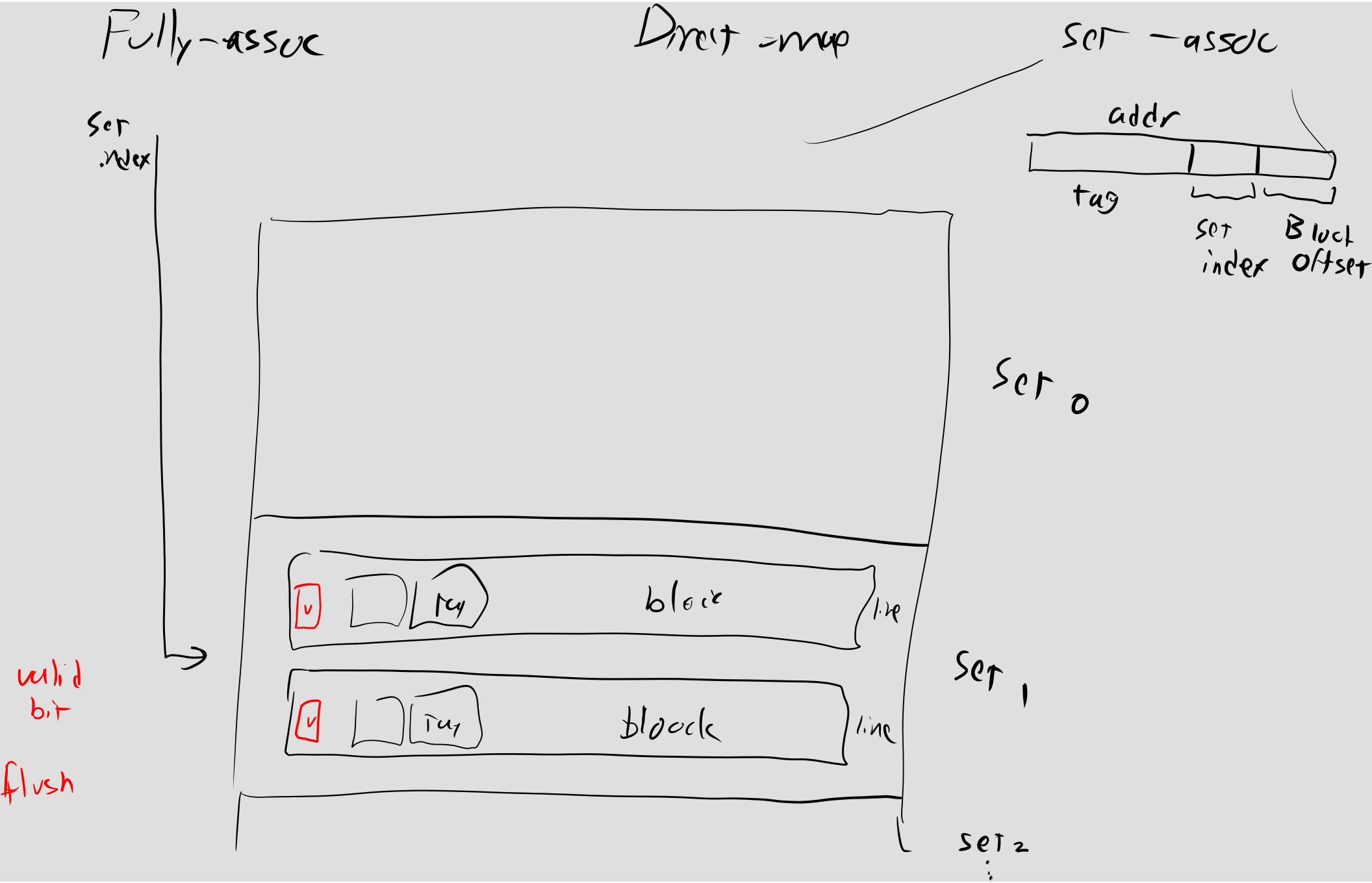
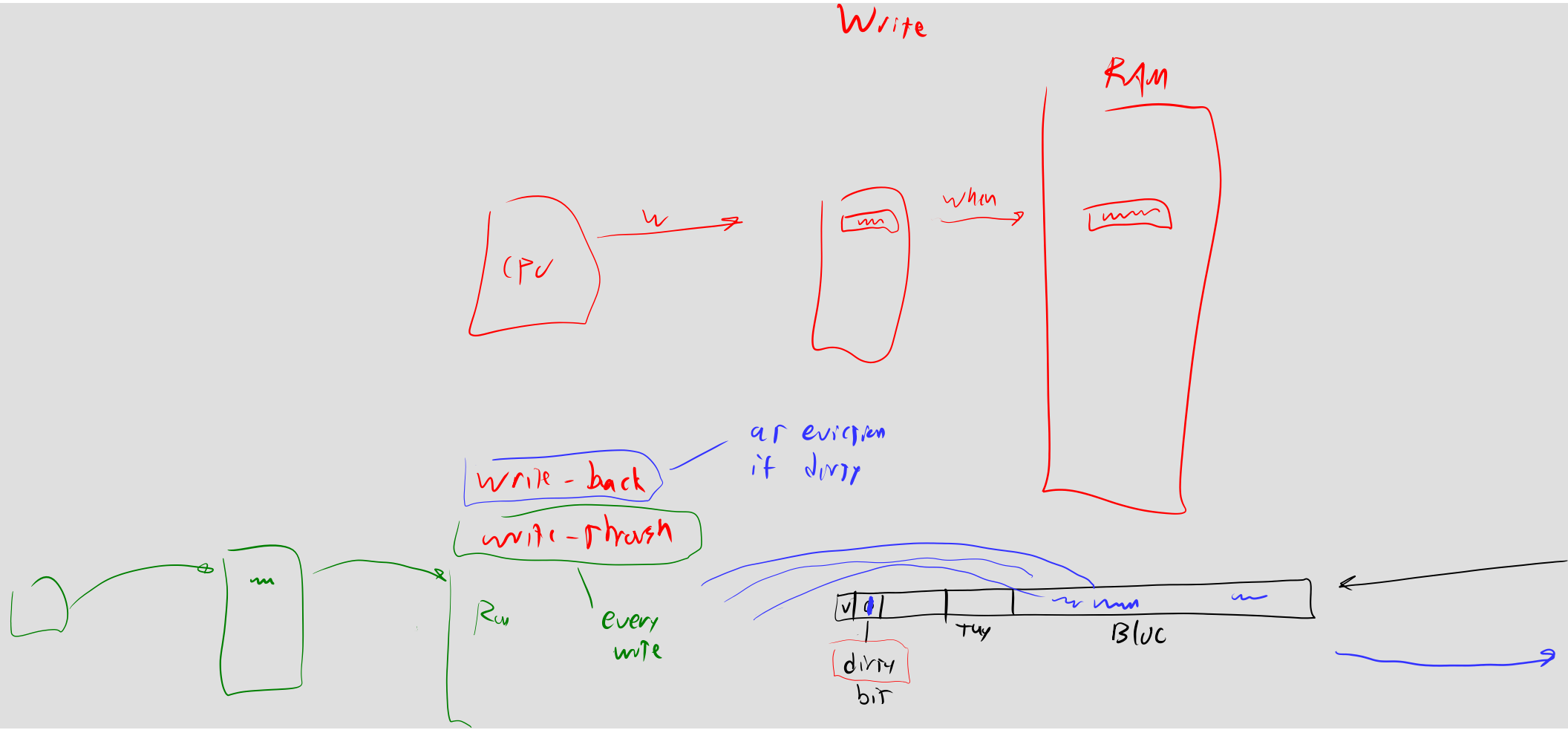
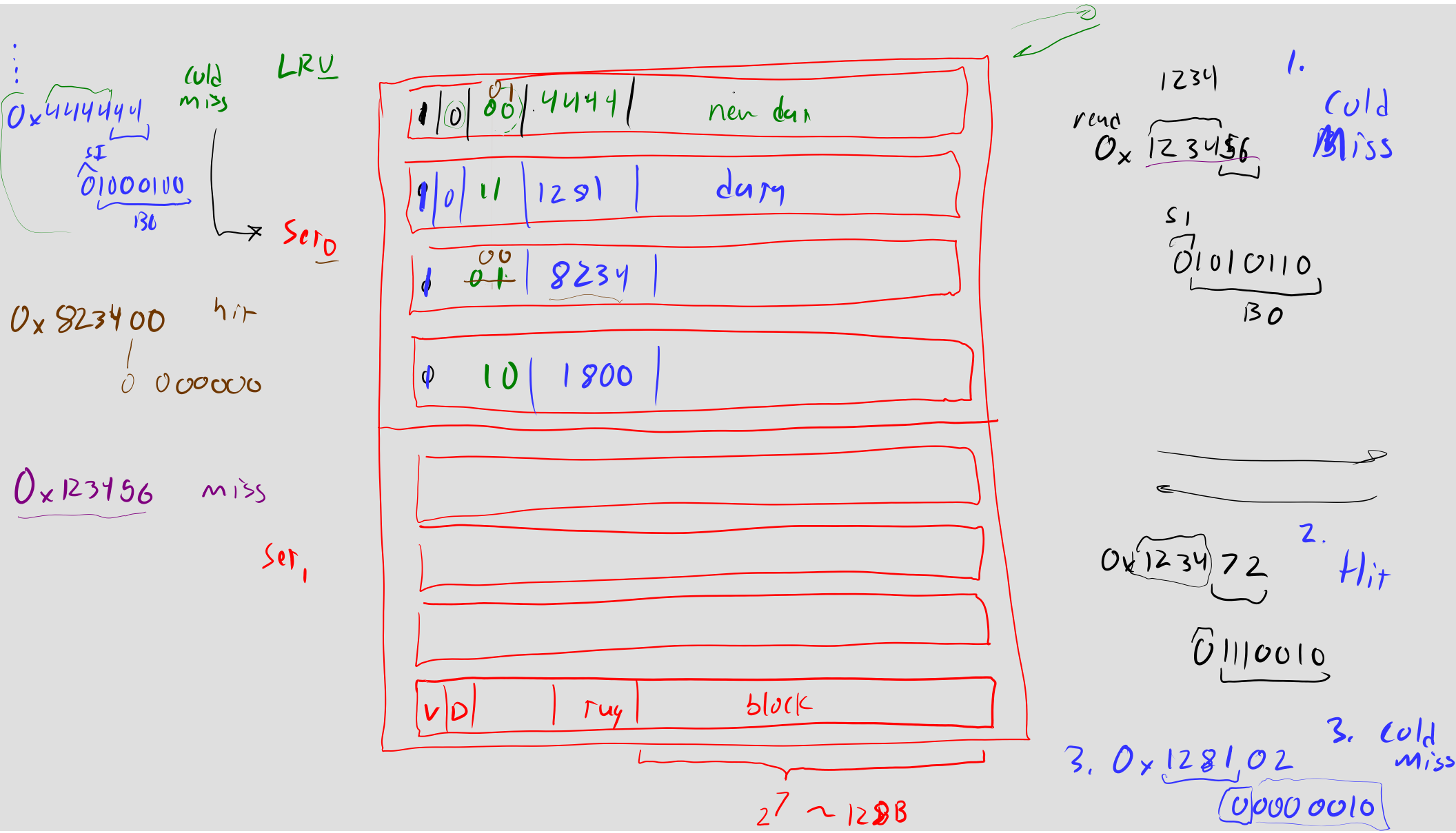
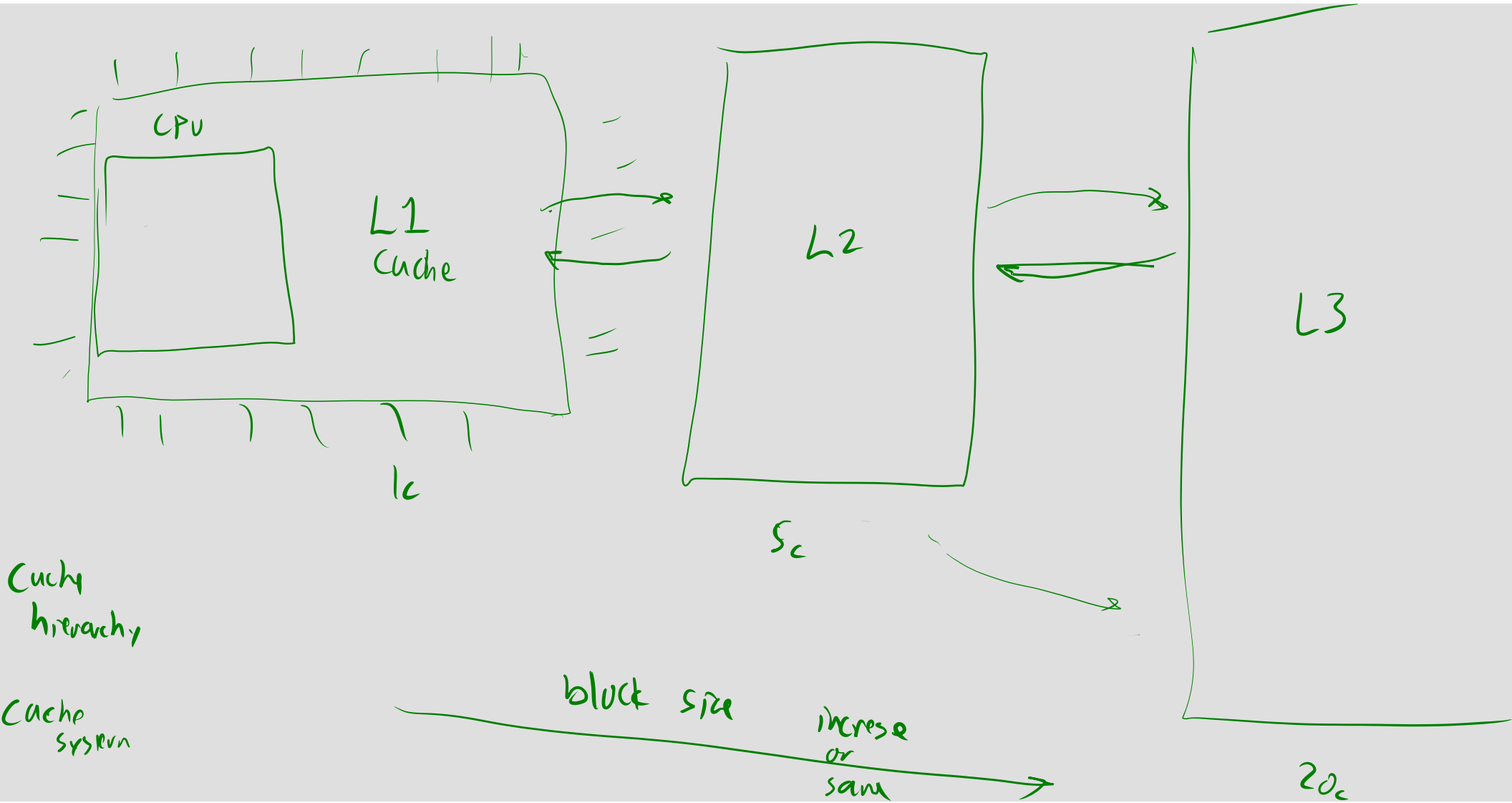

Locality
LRU
Temp
Spat
CPU
replace
Cache
RAM
block
Tag
line


Fully-assoc
Direct-map
set-assoc
addr
tag
set index
Block offset
set
index
valid bit
flush
v
tag
block
line
set 0
set 1
set 2


Write
RAM
CPU
when
write-back
at eviction
if dirty
write-through
every
write
Row
tag
block
dirty
bit


LRU
cold miss
0x444444
01000100
set
130
set0
0x823400
hit
0 000000
0x123456
miss
set1
1 0 00 4444
new data
1 0 11 1291
dirty
1 01 8234
1 10 1800
v d tag block
2^7 ~ 128B
1.
1234
read
0x 123456
cold Miss
s1
01010110
130
2.
0x 1234 72
hit
01110010
3. 0x 128102
3. cold miss
00000010

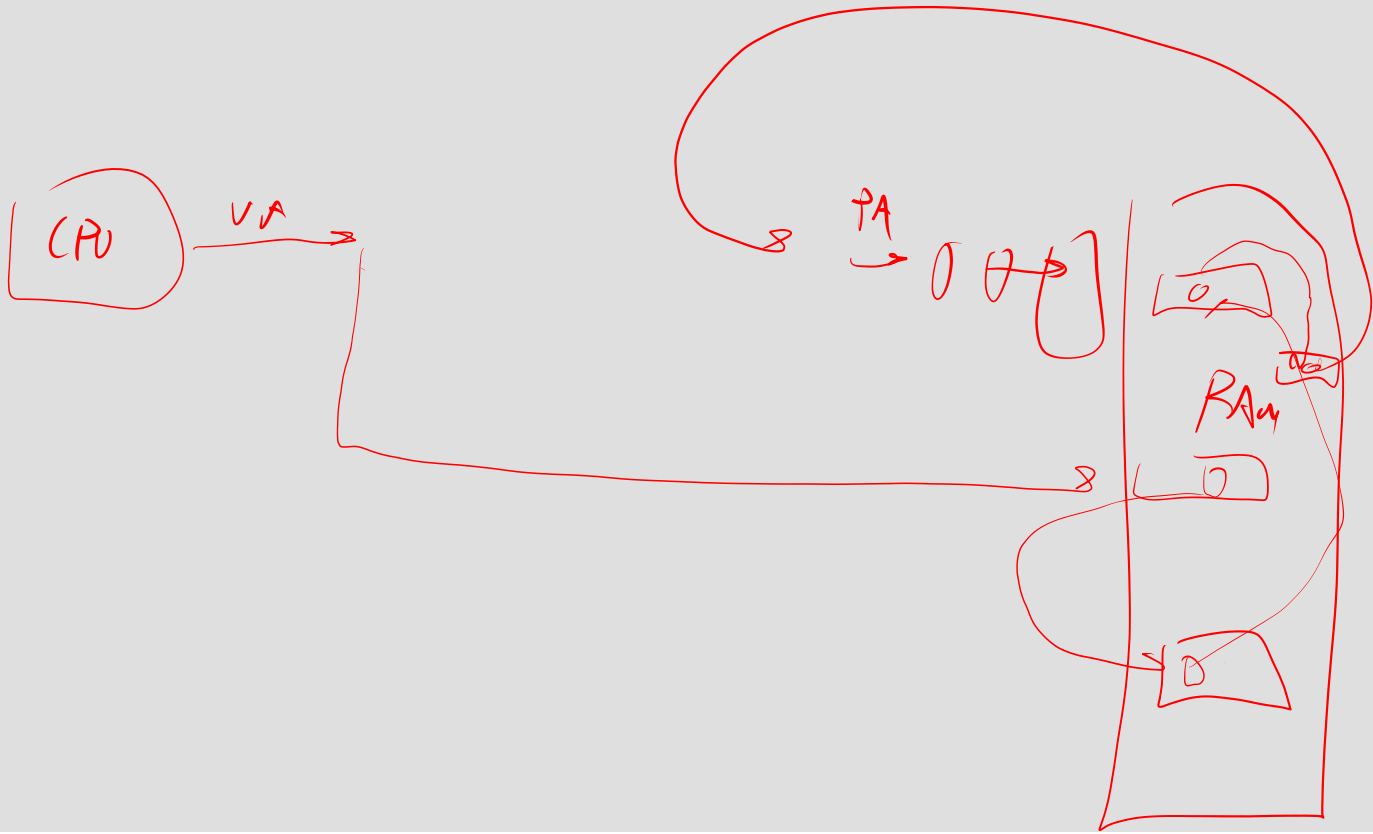

CPU
L1
Cache
L2
L3
1c
5c
20c
Cache hierarchy
Cache system
block size
increase or same

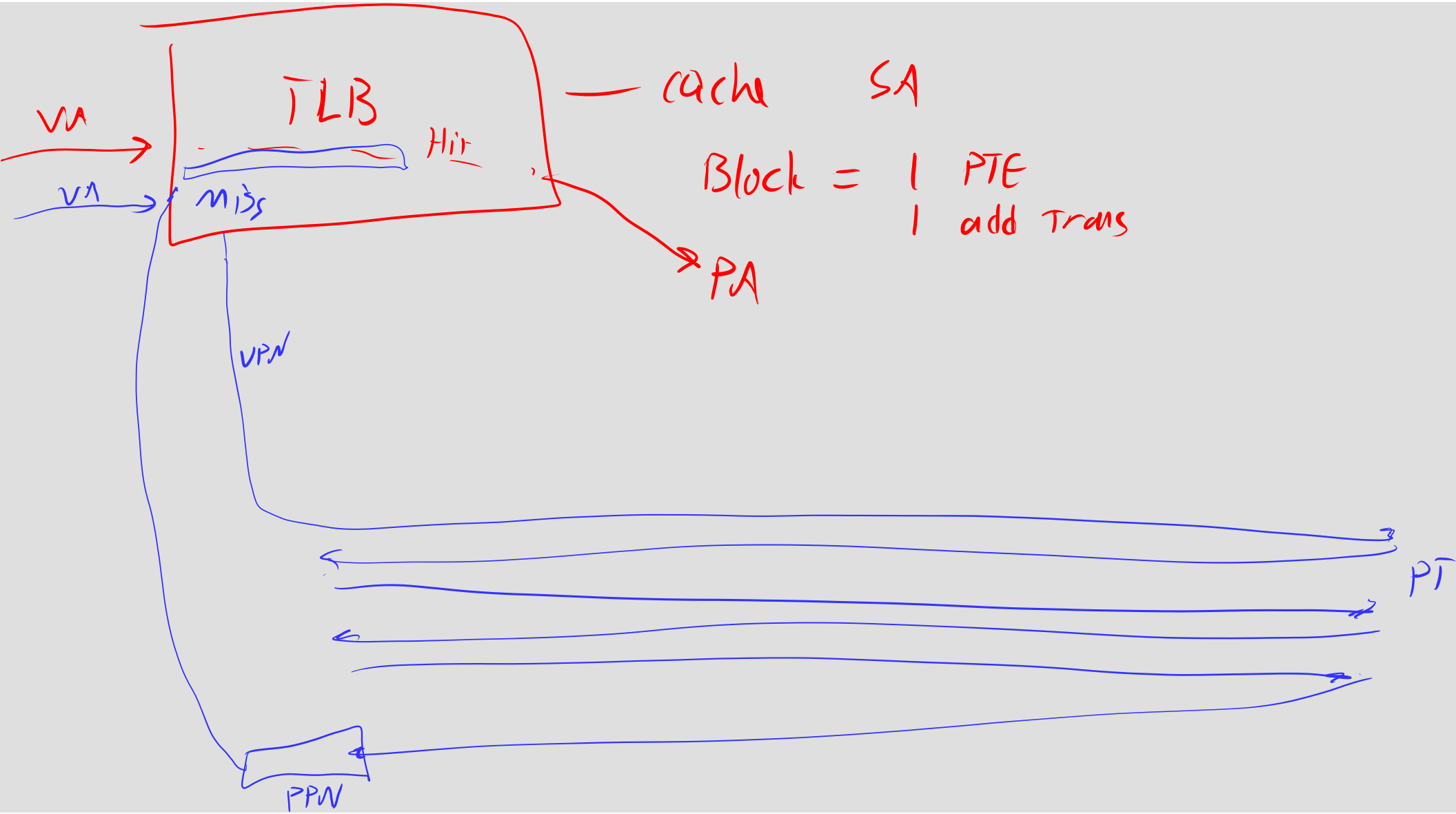
Translation → Page table VA → PA

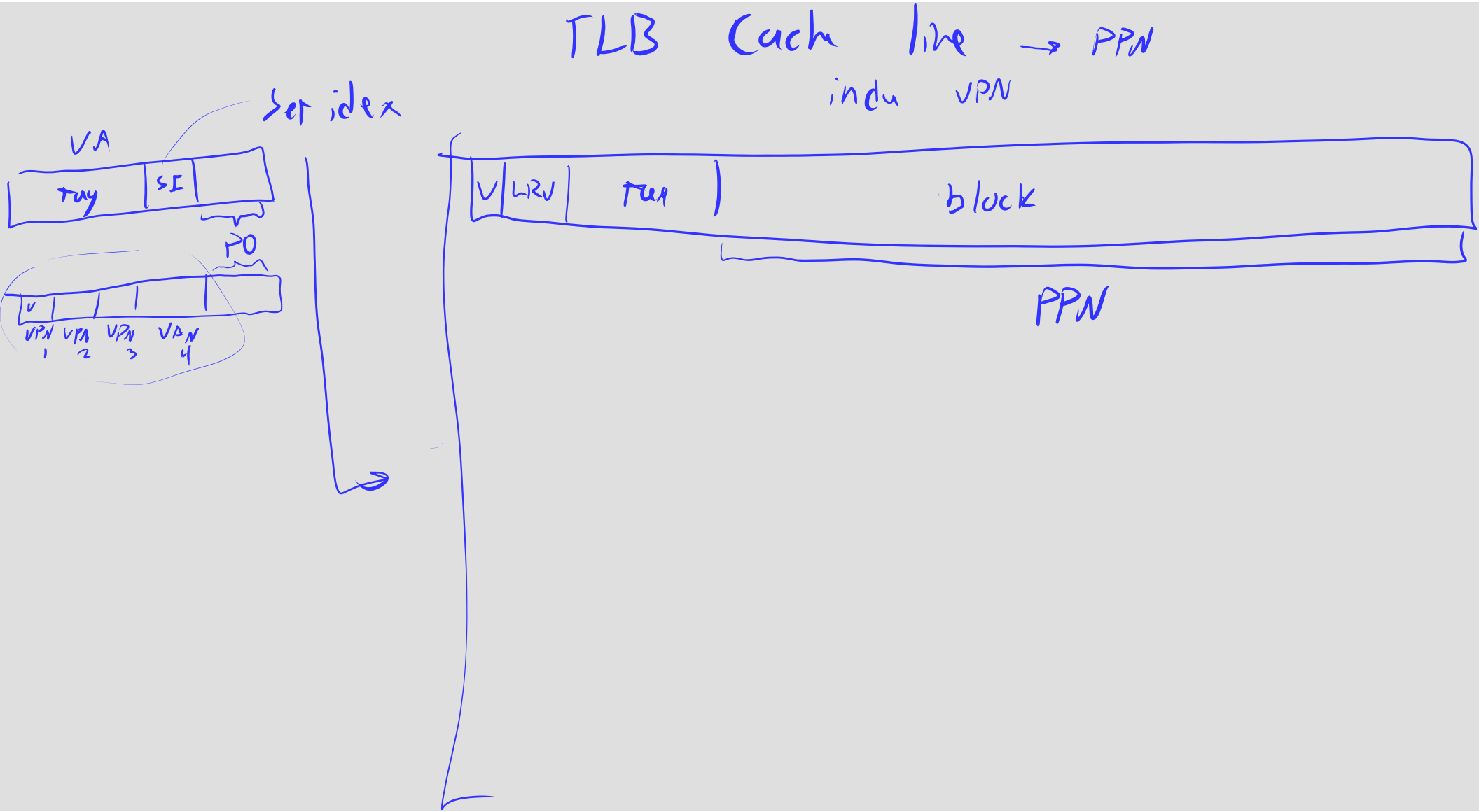
Lookaside

Buffer → cache

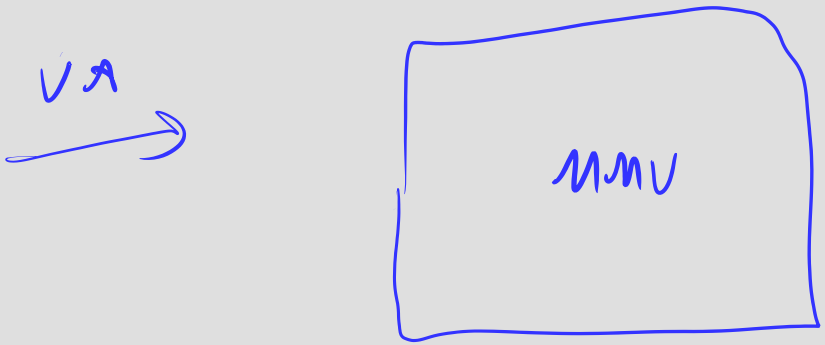
TLB




TLB
cache
SA
VA
VA
Hit
misS
Block = 1 PTE
1 add Trans
PA
VPN
PT
PPN


TLB Cach line → PPN
indu VPN
Set idex
VA
tag
SI
PO
V
VPN 1
VPN 2
VPN 3
VPN 4
V
LRU
tag
block
PPN

Memory Management Unit



1. sep. Tag, SI, PO
2. check TLB
   - Hit? TLB PPN : PO → address
   - Miss? 3. Split VPN
     4. check PTBR
     5. ... ...
     ... ...
     ... ...

n. PPN → TLB

n+1. PPN : PO → address