Q

Caches — where TLB re L#

Why scan thru

back — next cache

↳ dirty

TLB arguss —— PPN ~ PTE / Protectionbit

how updat multiple caches fast —— research Q

LL v Arm re temporal locality

2 type locality

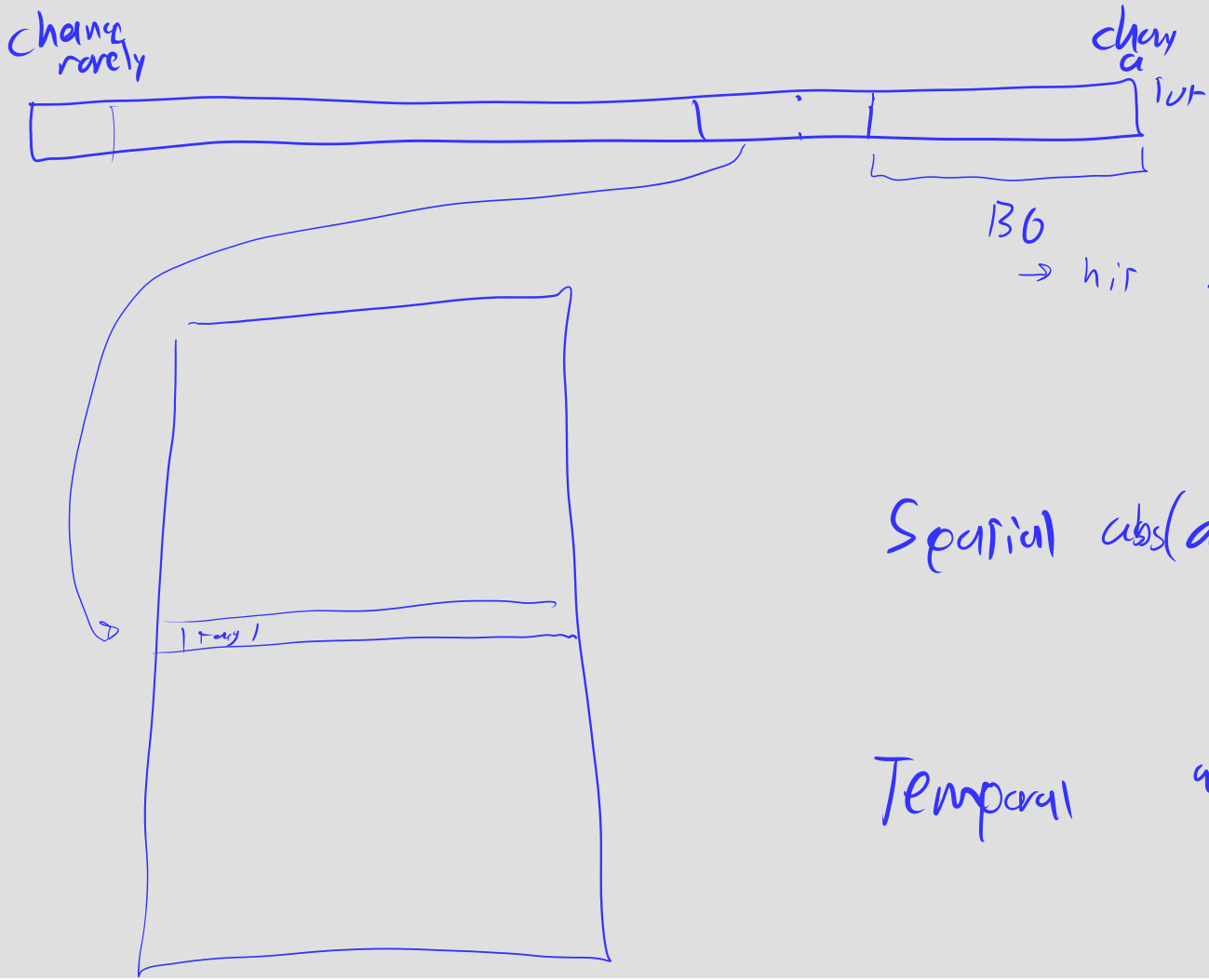
Why tag?

val	PTR

ll[100]

Tag
SI
BO

Spatial locality

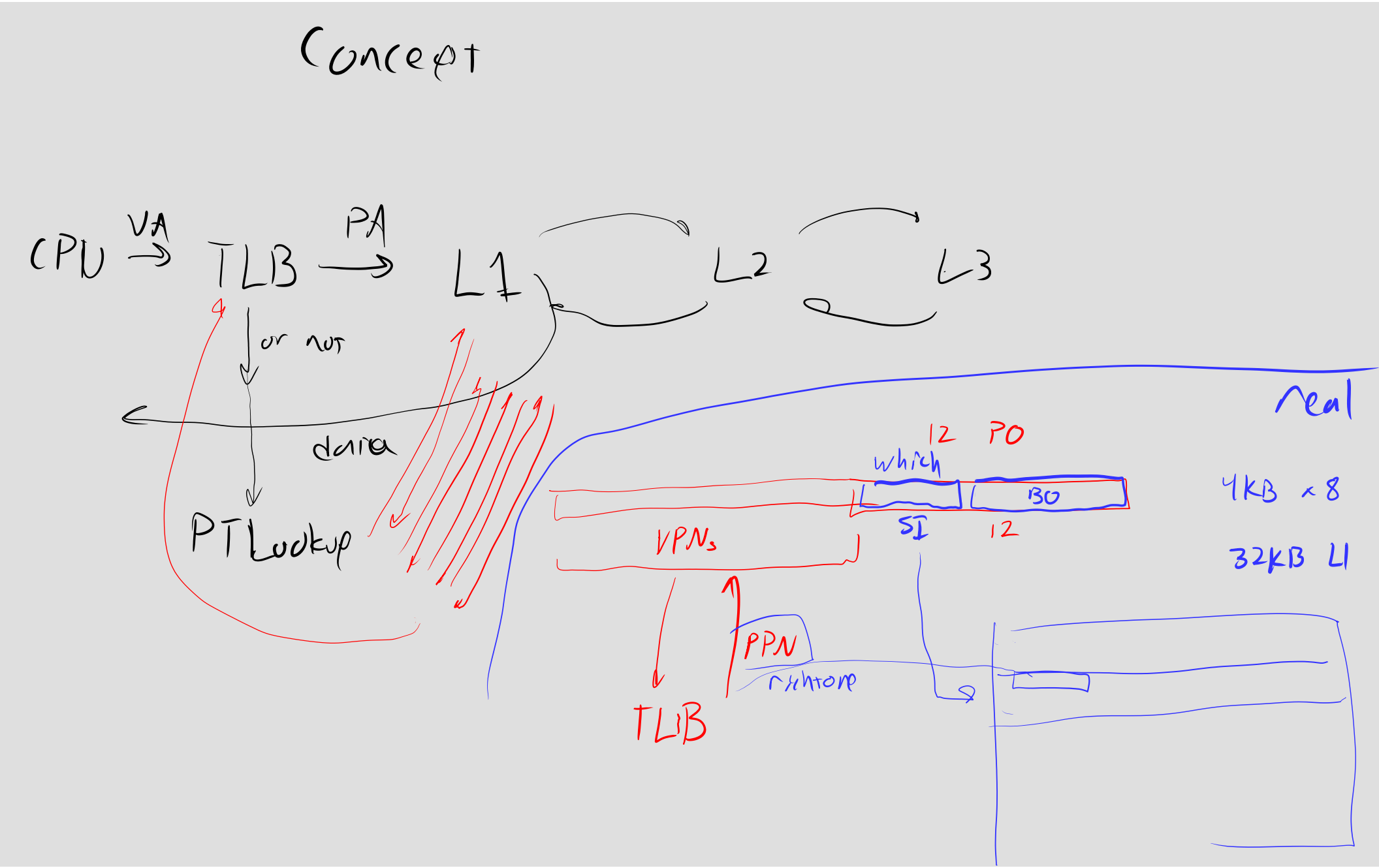


→ hit spatial local

Spatial $abs(addr_i - addr_{i-1})$ small

Temporal $addr_i = addr_{i+n}$ for many i, small n

Concept


CPU
VA
TLB
PA
L1
L2
L3
or not
data
PTLookup
real
12
PO
which
130
SI
12
VPNs
PPN
TLB
4KB x 8
32KB L1

Process — each has own addr space

OS

interruptible

Thread — all share same addr space, file descr

each has own prog registers

OS / H/W

interruptible

fiber / greenlet — all share everything

Coroutines

user-space

non interruptible