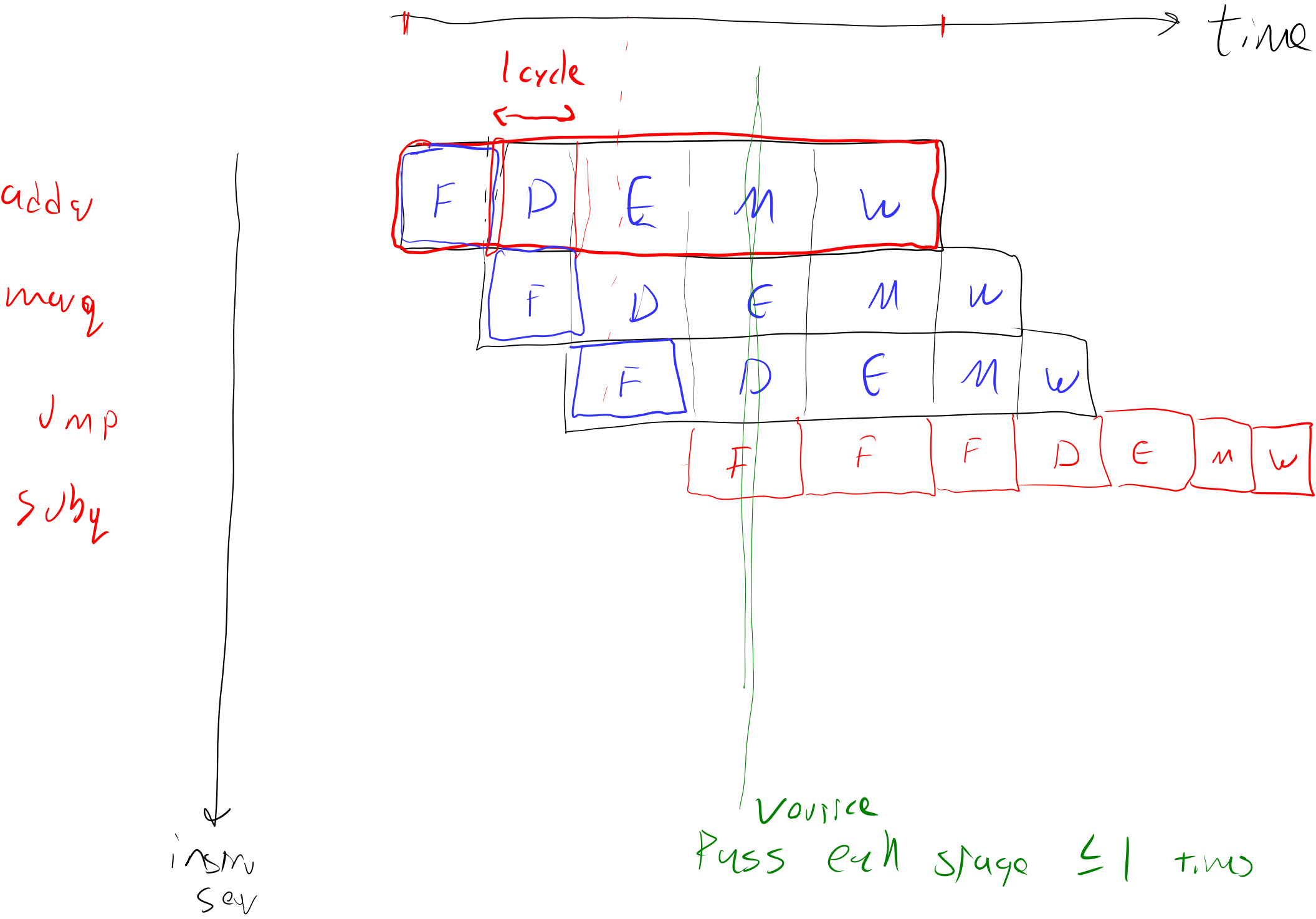
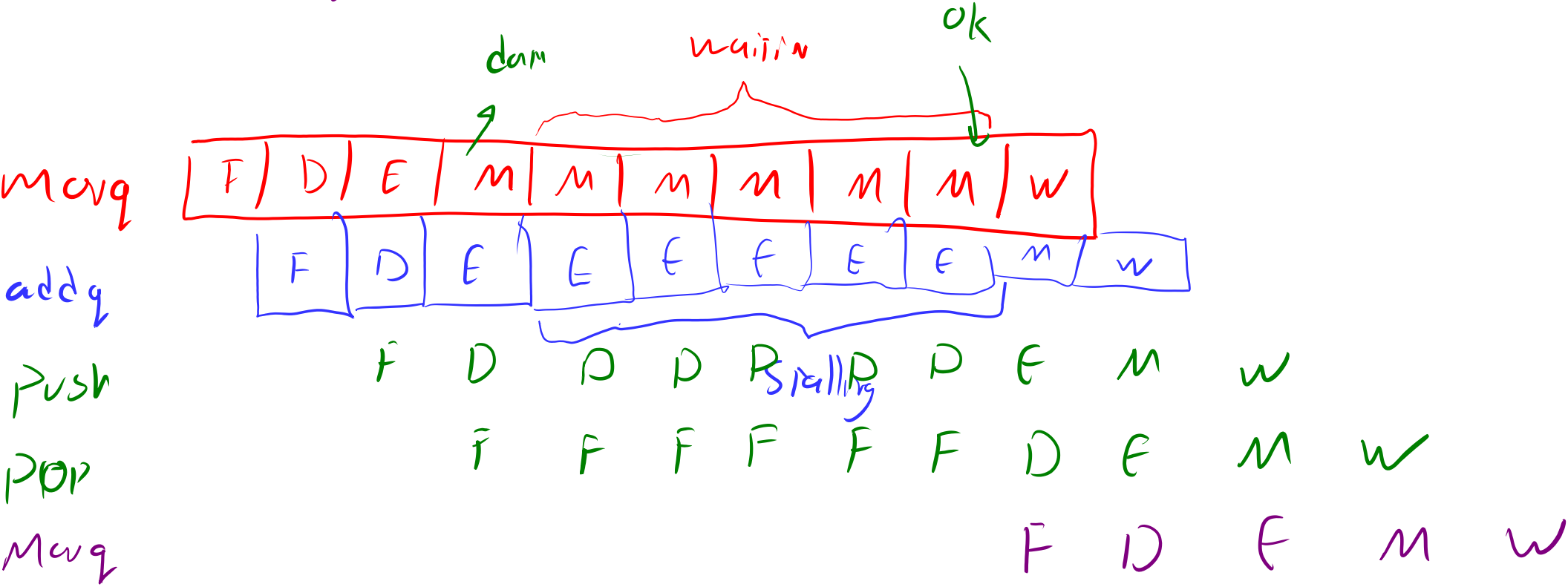

The End
is
Nigh!


time
1 cycle
add q
mul q
jmp
sub q
F D E M W
F D E M W
F D E M W
F F F D E M W
insn seq
Source
Pass each stage ≤ 1 time

```
movq (%rax), %rdx
add  $3, %rdi
push %rdi
pop  %rsi
movq %rsi, %rd
```

	hit	cycle
L1		1
L2		5
L3		20
DRAM		300



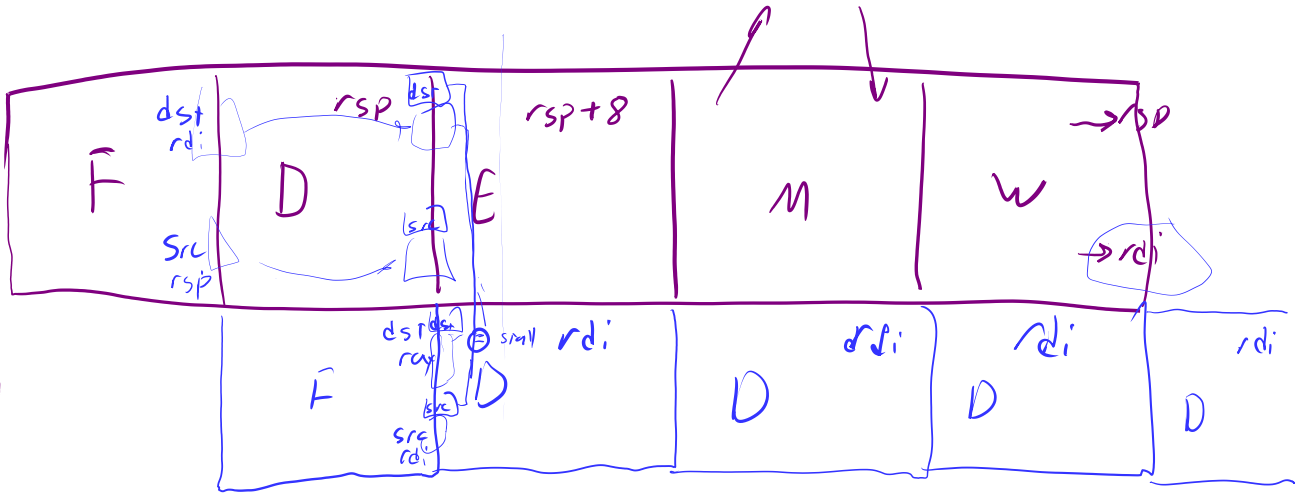
dura dep
→ small

addq $8 %rsp
movq (%rsp), %rdi

popq %rdi

movq (%rdi), %rax

dura dep



addq $8 %rsp
movq (%rsp), %rdi

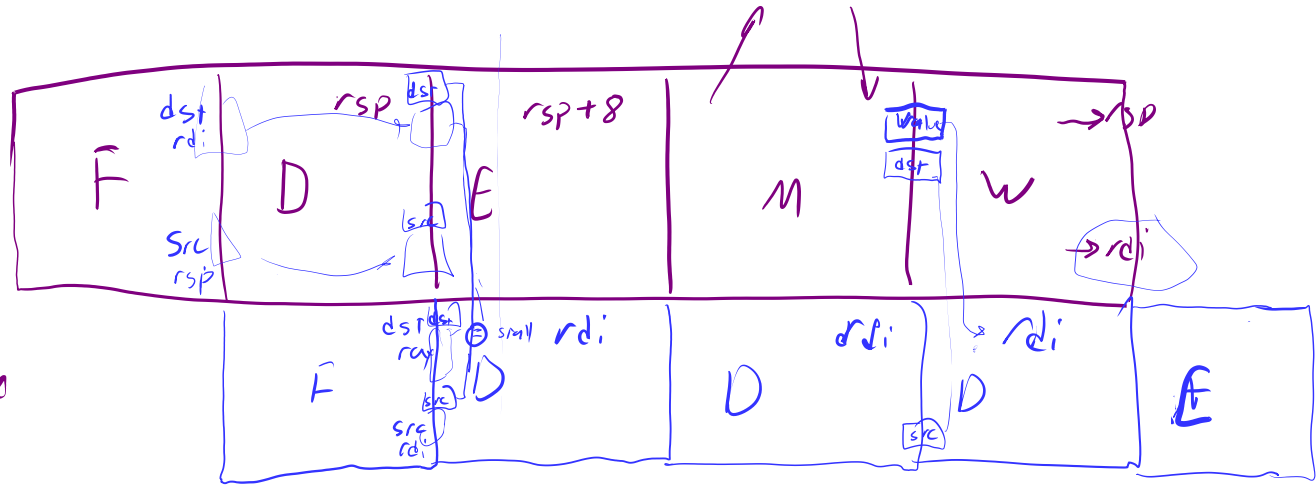
popq %rdi

movq (%rdi), %rax

data dep

→ ~~stall~~

Forward



Stall

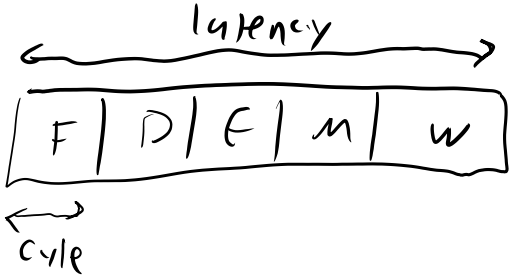
- by staying in stage
- why?
  a. the instruct before stalled
  b. Work is slow
  c. data dep ⟶ forward

- How know
  a. signal (wire) tells us
  b. Function Unit tells us
  c. Compare pipeln reg

Forward

- how? Comp pipeln reg

latency $STOP_{time} - START_{time}$



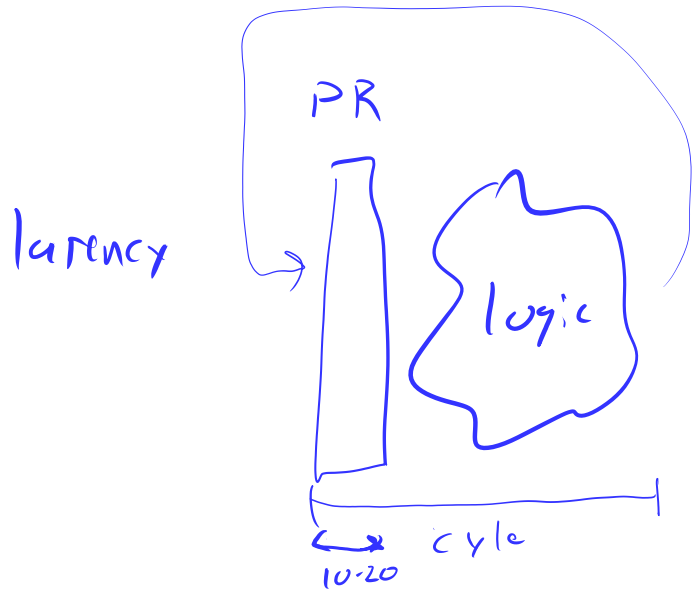
Throughput $\frac{\text{things}}{\text{time}} \approx \frac{1}{\text{cycle}}$

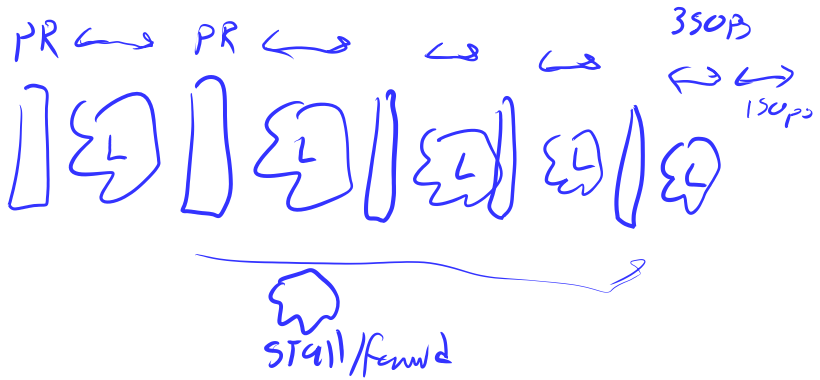
$\frac{1}{s} = Hz$

$\frac{1}{2{,}000{,}000{,}000} GHz$

Pipeline increase both!

$500\ ps$





ALU

int

+

1cy

fp

+

3cy

I d

3-30 cycles