Evaluating Overheads of Multi-bit Soft Error Protection Techniques at Hardware Level

Problem-Motivation-Approach

Problem

- As devices become smaller, particle strike radius affects more circuit components.
- In addition to storage (SRAM) circuits, it is now becoming a concern for logic (combinational/sequential) components.
- Single particle strikes can cause a multi-bit soft error that affects bits in the same or adjacent components.

Motivation

- Traditional techniques for single-bit soft errors in logic do not provide satisfactory protection against multi-bit errors.
- We need to evaluate more aggressive techniques as they significantly change the overhead of protection.
- We evaluate:
  - SECED (Single Error Correction, Double Error Detection)
  - Error Correcting Codes
  - Spatial Redundancy
  - Temporal Redundancy

Approach

- Use example processor design
  - OpenRISC 1000:
    - Area, power, speed, etc.
    - Microarchitectural details
    - Design principles and design details

- Design protection scenarios in terms of
  - Area
  - Average Power

Soft Error Protection

Types of Circuits

- Fine-grained Techniques
  - SECED (Single Error Correction, Double Error Detection)
  - Error Correcting Codes
  - Spatial Redundancy
  - Temporal Redundancy
- Coarse-grained Techniques
  - Cycle-level Spatial Redundancy
  - Multi-cycle-level Spatial and Temporal Redundancy

Area Overhead

- Component-level

- Spatial Redundancy
  - SECED offers protection for storage elements at low overhead, therefore it is preferred by IBM (SECED) and Intel (RIMI).
  - Spatial Redundancy is optimal for logic circuits, where it protects both sequential and combinational logic on an overhead lower than that of SECED.

- Delay and Power Overhead

- Component-level

- Spatial Redundancy
  - Granularity does not affect the overall delay, as there is still the same amount of logic in the critical path.
  - Power overhead of Spatial Redundancy slightly decreases at higher granularity due to the smaller number of storage elements protected.

Design Scenarios

- Designs that use SECED codes for storage (SRAM) circuits and Spatial Redundancy for logic (combinational/sequential) circuits.

- Area can be traded for performance by checking correctness at multi-cycle time scale (100 cycles, for example).
- Performance can be traded for area by performing redundant computation in parallel under Temporal Redundancy.

- Designs that use Reed-Solomon codes for the lowest component (SRAM) in the shortest overall delay.
- Checking correctness at a multi-cycle time scale can be done in the critical path, thus shortening the overall delay.
- Designs that recognize the use of SECED for logic circuits achieve the lowest power consumption.

Lessons and Future Goals

- Lessons Learned
  - Multi-bit soft errors are becoming a concern in logic (combinational/sequential) circuits.
  - Protection against multi-bit errors in logic components requires techniques that are more aggressive than traditionally used parity approaches.
  - Error detection/correcting codes are preferred for storage (SRAM) circuits while Spatial Redundancy is preferred for logic (combinational/sequential) circuits.
  - Improved protection granularity of Spatial Redundancy only slightly increases overhead when traded for performance.
  - Area can be traded for performance by checking correctness in parallel under Temporal Redundancy.

- Future Goals
  - Use error injection in the simulator to evaluate granularity of and effectiveness of protection techniques.
  - Evaluate performance and power for common benchmarks.
  - Investigate recovery overhead of protection mechanisms.
  - Consider wider range of protection techniques.
  - Evaluate benefit of multi-cycle Temporal Redundancy in a superscalar processor at application level.

Project Information

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- Technology Transfer

- Lessons from the project and their impact on the industry.
- Would like to identify new technology transfer opportunities.