Saturday, September 16

8:30-5:30  **Workshop 1:** Programming Models for Ubiquitous Parallelism  
Sam Midkiff, Purdue  
Maria Garzaran, Illinois

8:30-12:30  **Tutorial 1:** Cell BE Processor: Programming Tools and Techniques  
Michael Perrone and Kathryn O’Brien, IBM Research

12:30-1:30  **Lunch**

1:30-5:30  **Workshop 2:** MEDEA-7: MEmory Performance: DEaling with Applications, systems, and architecture  
Cosimo Antonio Prete and Pierfrancesco Foglia, University of Pisa  
Sandro Bartonlini, University of Siena

**Tutorial 2:** A Case Study of a Physically Based Visual Simulation Targeting Emerging Architectures and Programming Models  
Yahya Mirza, Aurora Borealis Software LLC

Sunday, September 17

8:30-12:30  **Workshop 3:** TCHA: Tools and Compilers for Hardware Acceleration  
Walid Najjar, UC-Riverside  
Kathryn O’Brien, IBM Research

**Tutorial 3:** X10: Concurrent Object-Oriented Programming for Modern Architectures  
Vijay Saraswat and Christoph von Praun, IBM Research

**Tutorial 5:** IA-32 Execution Layer: Dynamic Binary Translator from IA32 to Intel Itanium Architecture  
Orna Etzion and Yigal Zemach, Intel

12:30-1:30  **Lunch**

1:30-5:30  **Workshop 4:** 2nd Intl Workshop on Operating System Interference in High Performance and Parallel Applications  
Ronald Mraz, Owl Computing Technologies,  
Fabrizio Petrini, Pacific Northwest National Laboratory  
Matt Sottile, Los Alamos National Laboratory

**Tutorial 4:** Transactional Programming in a Multi-Core Environment Targeting Emerging Architectures and Programming Models  
Bratin Saha and Ali-Reza Adl-Tabatabai, Intel  
Christos Kozyrakis, Stanford
**Monday, September 18**

8:15-8:30  *Opening Remarks*

8:30-9:30  **Keynote I:** Jeff Dean, Google  
*Experiences with MapReduce, an Abstraction for Large-Scale Computation*

9:30-10:00  **Break**

10:00-11:30  **Track 1 (Session 1): Multi-core Design I**  
*Architectural Support for Operating System-Driven CMP Cache Management*  
- Nauman Rafique, Won-Taek Lim, Mithuna Thottethodi  
*Communist, Utilitarian, and Capitalist Cache Policies on CMPs: Caches as a Shared Resource*  
- Lisa R. Hsu, Steven K. Reinhardt, Ravishankar Iyer, and Srihari Makineni  
*Core architecture Optimization for Heterogeneous Chip Multiprocessors*  
- Rakesh Kumar, Dean M. Tullsen, and Norman P. Jouppi

**Track 2 (Session 2): Program Analysis and Optimization**  
*Compiling for Stream Processing*  
- Abhishek Das, William J. Dally, and Peter Mattson  
*Region Array SSA*  
- Silvius Rus, Guobin He, Christophe Alias, and Lawrence Rauchwerger  
*A Two-Phase Escape Analysis for Parallel Java Programs*  
- Kyungwoo Lee and Samuel P. Midkiff

11:30-12:30  **Lunch**

12:30-5:30  **Excursion to Boeing Plant -- Sponsored by AMD**

5:30  **Arrival back in Seattle / Dinner on your own**
Tuesday, September 19 Morning

8:30-9:30  **Keynote II**, Steve Scott, Cray

9:30-10:00  **Break**

10:00-11:30  **Track 1** (Session 3): **Security and Correctness**

- **Self-Checking Instructions -- Reducing Instruction Redundancy for Concurrent Error Detection**
  - Sumeet Kumar and Aneesh Aggarwal

- **A Low-cost Memory Remapping Scheme for Address Bus Protection**
  - Lan Gao, Jun Yang, Marek Chrobak, Youtao Zhang, San Nguyen, and Hsien-Hsin S. Lee

- **Efficient Data Protection for Distributed Shared Memory Multiprocessors**
  - Brian Rogers, Milos Prvulovic, and Yan Solihin

**Track 2** (Session 4): **Characterizing Program Behavior**

- **Wavelet-Based Phase Classification**
  - Ted Huffmire and Tim Sherwood

- **Complexity-based Program Phase Analysis and Classification**
  - Chang-Burm Cho and Tao Li

- **Performance Prediction based on Inherent Program Similarity**
  - Kenneth Hoste, Aashish Phansalkar, Lieven Eeckhout, Andy Georges, Lizy K. John, and Koen de Bosschere

11:30-12:30  **Lunch -- Sponsored by Sony**
**Tuesday, September 19 Afternoon**

12:30-1:30  *Keynote III*, Ajay Royyuru, IBM  
*Deep Computing in Biology: Challenges and Progress*

1:30-2:00  *Break*

2:00-3:30  **Track 1** (Session 5):  **Multi-core Design II**  
*Hardware Support for Spin Management in Overcommitted Virtual Machines*  
- Philip M. Wells, Koushik Chakraborty, and Gurindar S. Sohi  
*Testing Implementations of Transactional Memory*  
- Chaiyasit Manovit, Sudheendra Hangal, Hassan Chafi, Austen McDonald, Christos Kozyrakis, and Kunle Olukotun  
*Efficient Emulation of Hardware Prefetchers via Event-Driven Helper Threading*  
- Ilya Ganusov and Martin Burtscher

**Track 2** (Session 6):  **Performance Profiling and Tuning**  
*DEP: Detailed Execution Profile*  
- Qin Zhao, Joon Edward Sim, Weng-Fai Wong, and Larry Rudolph  
*Whole-Program Optimization of Global Variable Layout*  
- Nathaniel McIntosh, Sandhya Mannarswamy, and Robert Hundt  
*Fast, Automatic, Procedure-Level Performance Tuning*  
- Zhelong Pan and Rudolf Eigenmann

3:30-4:00  *Break*

4:00-5:30  **Track 1** (Session 7):  **Instruction Fetch and Control Flow**  
*Reducing Control Overhead in Dataflow Architectures*  
- Andrew Petersen, Martha Mercaldi, Steve Swanson, Andrew Putnam, Andrew Schwerin, Mark Oskin, and Susan Eggers  
*Power-efficient Instruction Delivery through Trace Reuse*  
- Chengmo Yang and Alex Orailoglu  
*Branch Predictor Guided Instruction Decoding*  
- Oliverio J. Santana, Ayose Falcon, Alex Ramirez, and Mateo Valero

**Track 2** (Session 8):  **Application-Specific Optimizations**  
*Two-level Mapping based Cache Index Selection for Packet Forwarding Engines*  
- Kaushik Rajan and R. Govindarajan  
*Program Generation for the All-Pairs Shortest Path Problem*  
- Sung-Chul Han, Franz Franchetti, and Markus Pueschel  
*Combining Analytical and Empirical Approaches in Tuning Matrix Transposition*  
- Qingda Lu, Sriram Krishnamoorthy, and P. Sadayappan

6:00-8:00  *Reception / Dinner -- Sponsored by CA*
Wednesday, September 20

8:30-9:30  **Keynote IV**, David Kirk, Nvidia

9:30-10:00  **Break**

10:00-11:30  **Track 1** (Session 9): **Out-of-order Microarchitecture**
* Adaptive Reorder Buffers for SMT Processors
  - Joseph Sharkey, Deniz Balkan, and Dmitry Ponomarev
  * **SEED: Scalable, Efficient Enforcement of Dependencies**
  - Francisco J. Mesa-Martinez, Michael C. Huang, and Jose Renau
  * **SPARTAN: Speculative Avoidance of Register Allocations to Transient Values for Performance and Energy-Efficiency**
  - Deniz Balkan, Joseph Sharkey, Dmitry Ponomarev, and Kanad Ghose

11:30-11:45  **Concluding Remarks**