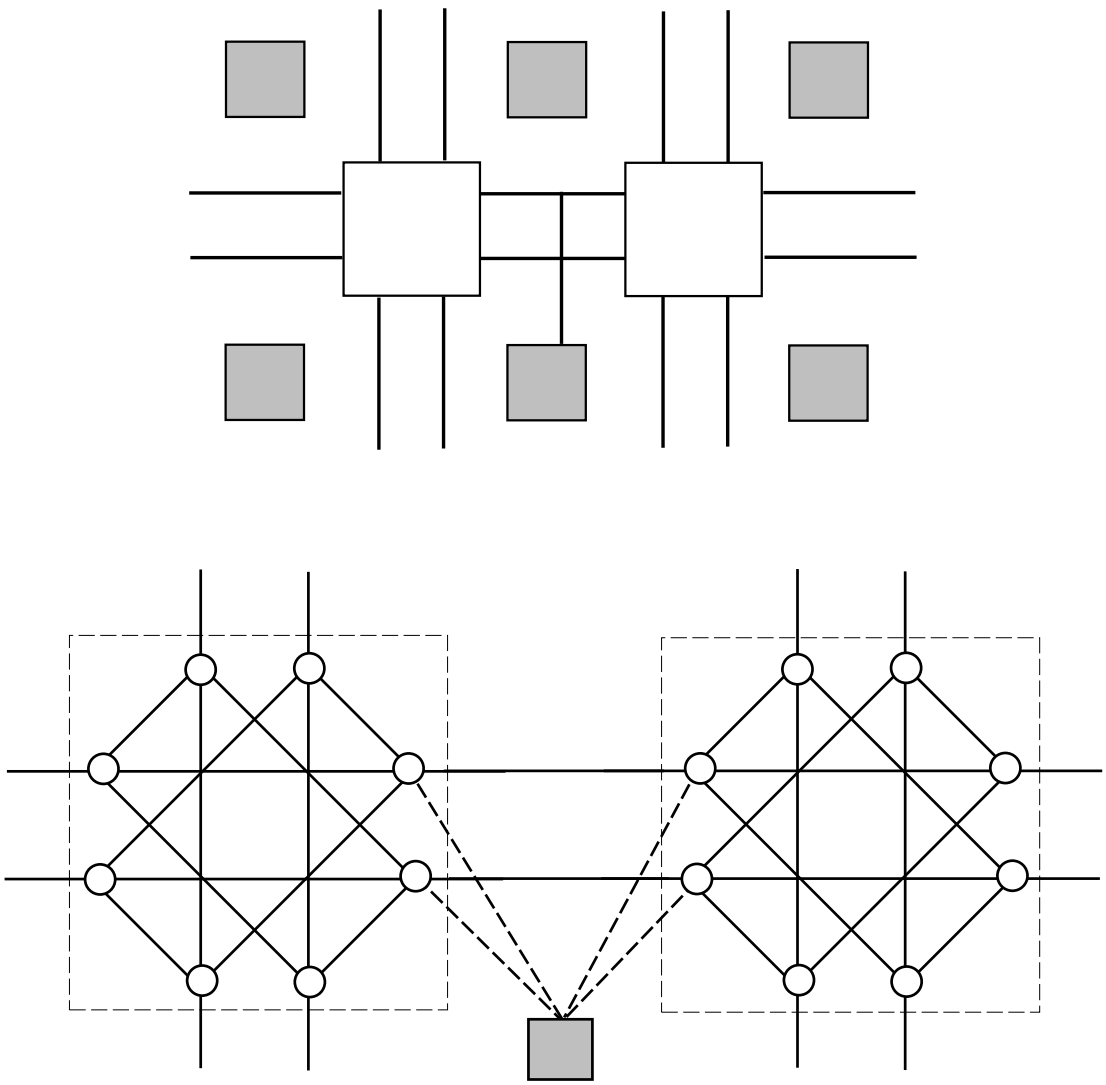

Figure 2. An FPGA routing graph model.