Closing the Power Delivery/Heat Removal Cycle for Heterogeneous Multi-Scale Systems

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Abstract

The semiconductor industry is poised to continue the historic Moore's law trend of doubling the level of integration every 1.5-2 years, even as the virtuous cycle benefits of Dennard scaling are quickly vanishing. Once devices no longer scale laterally, the only way to continue to increase areal density is by going vertical using 3D-IC. However, 3D-IC raises several fundamental difficulties in addition to the clear fabrication challenges: as the number of physical layers in a 3D-IC stack increases, from the present 2.5D multi-layer solutions (with an interposer, or only a couple of layers), to true 3D many-layer stacks, the energy cycle problem of delivering power to and removing heat from the 3D stack become daunting. The main reason for this power wall is the mismatch between the volumetric (cubic) power consumption and heat dissipation in 3D-IC, and the areal (quadratic) power delivery and heat removal through a 2D surface (top and/or bottom of the stack). In this paper we propose MultiSpot, a framework to provide fundamental solutions to the 3D-IC power wall that are also practical.

1 Moore's law through 3D-IC

The semiconductor industry is poised to continue the historic Moore's law trend of doubling the level of integration every 1.5-2 years, even as the virtuous cycle benefits of Dennard's scaling (devices get simultaneously smaller, faster and lower power) are quickly vanishing or have already stopped. Once devices no longer scale laterally (Dennard scaling stops), one way to continue to increase density is by going vertical as three-dimensional integrated circuits (3D-IC) which can be monolithic (e.g. 3D-NAND Flash), or through-Silicon via (TSV)-based; but 3D-IC raises several fundamental difficulties in addition to the clear fabrication challenges. As the number of physical layers in a 3D-IC stack increases, from the present 2.5D multi-layer solutions, with an interposer, or only a couple of layers, to true 3D many-layer stacks, the energy cycle problem of delivering power to, and removing heat from, the 3D stack become daunting. The main reason for this power wall is the mismatch between the volumetric (cubic) power consumption and heat dissipation in 3D-IC, and the areal (quadratic) power delivery and heat removal through a 2D surface (top and bottom of the stack).

1.1 3D-IC as an enabler for Moore's Law

Moore's original observation that later became a "law" had to do only with the exponential increase in the number of transistors that can be economically integrated in a single chip. The later various flavours of "Moore's laws" (e.g. exponential increases in performance, decreases in power, etc.) have been just a by-product of the way the semiconductor industry was able to stay on the Moore's law path by using transistor scaling rules first proposed by Dennard. Today Dennard scaling has reached several "red brick walls" – lateral overall transistor dimensions and power supply voltages scale at slower rates, if at all, thus clock rates and power densities are essentially staying constant – yet Moore's law in its originalist form (i.e. exponential increase in level of integration) is poised to continue, with 3D-IC as an essential mechanism for staying on the historical integration trend. There are several major advantages of 3D-IC: 1) reduction of average wirelength from a square root of lateral dimensions to a cubic root, 2) enabling heterogeneous architectures, heterogeneous technologies, such as CMOS and DRAM, 3) significant improvement of bandwidth and latency due to the availability of TSVs, 4) allowing low voltage and high power efficiency.

1.2 Power delivery and heat removal walls for 3D-IC

3D-IC is a general term that describes technologies that either use monolithic integration methods (e.g. 3D NAND Flash) or use several Silicon layers on top of each other (stacked 3D-IC) such that more transistors can be integrated in the same lateral footprint. For the purpose of this work we are interested in future trends thus we will focus on 3D-IC schemes that are scalable to many layers; such 3D-IC solutions will use a large number of thinned Silicon layers that are connected to each other using through-Silicon vias (TSVs). Since these are true three-dimensional structures, power is usually delivered using controlled-collapse chip connections (C4s) on one side of the 3D stack (flip-chip), while heat is removed by a heat sink attached to the other side of the stack. To stay on the historical Moore's law trend will require the number of layers in the 3D-IC stack to increase, which means the power consumption and dissipation will increase in a cubic fashion (with the volume of the stack), while the power delivery and heat removal will be limited by the quadratic area of the top and bottom layers. Even without 3D-IC the number of power and ground pins and C4s on current chips is in the hundreds and can take more than half of the total number of pins, thus it is clear that simply trying to keep up by increasing the number of pins and C4s is unsustainable for 3D-IC. Similarly, the

thermal envelope limits of cooling are already stretched by current chips, alternative cooling solutions will be needed for 3D-IC.

1.3 Breaking the 3D-IC heat removal wall

3D-IC microchannel cooling offers a straightforward and efficient method to address the mismatch between volume and area by essentially offering some very low thermal impedance paths for the heat to travel from the inside of the 3D-IC stack to the outside. The heat transfer mechanism with microchannels is heat convection that is much more effective at removing heat than the heat conduction that would be the dominant mechanism in the stack without the microchannels. Regular liquid cooling on the top of the package also uses heat convection, but since it can only remove heat from the outside surface it does not resolve the mismatch – microchannels on the other hand, by traversing the actual volume of the 3D-IC stack can effectively "short-circuit" the high thermal impedance heat conduction paths, thus providing a fundamental solution.

1.4 Paper Objectives

Would concepts similar to the microchannel cooling work also for power delivery for 3D-IC? Can we use some form of low impedance paths to provide current to the interior of the 3D-IC volume? Interestingly, many decades ago the Cray-2 supercomputer did exactly that by using gold rods to provide power to a 3D stack made at the time of tightly integrated printed circuit boards.

The main objective of this paper and the recently started MultiSpot project is to provide fundamental solutions to the 3D-IC power wall that are also practical. The main hypotheses are that: 1) comprehensive solutions need to address both heat removal and power delivery synergistically, by closing the energy cycle, otherwise solutions become suboptimal, 2) since the brain is one of the main energy consumers in the body that also needs to be efficiently cooled, and since it potentially has the same volumetric vs. areal mismatch as future 3D-ICs, biology can provide useful inspiration for the problem at hand, and 3) design space exploration of the power delivery/heat removal problem requires tools that can model heterogeneous Systems-on-Chip (SoC) and Systems-on-Package (SoP).

1.5 Enhanced Micro-channels: Co-optimized simultaneous cooling and power delivery

The heat dissipation issue of 3D-IC arises from the increase of volumetric power density but decrease of the heat-dissipation surface area of the processors. The traditional air-cooling techniques heavily depend on the device-environment surface area and are obviously not adequate for 3D-IC. The emerging volumetric cooling technologies (e.g., micro-channel cooling) provide enough heat dissipation power to enable multi-layer 3D stacking. Pioneering studies have been done to investigate the effectiveness of liquid cooling for mitigating the thermal issues of 3D-IC. The results show that volumetric liquid cooling techniques, especially micro-channel cooling, extend the benefits of scaling for stacked processor and memory. Power efficiency can be further improved by optimizing the topology of micro-channels.

The power delivery issue is caused by the increasing power density, the increasing transistor-operation frequency and the decreasing operation voltage from technology scaling. High operation frequencies lead to even worse power delivery noise by increasing inductive voltage/power lost on the power delivery network (PDN). Decoupling capacitors (decap) are widely used as the major design-time technique to mitigate transient power delivery failures. A large amount of on-chip decap is desired to suppress the voltage supply noise under a given voltage variation level constraint. Larger decaps are needed to deal with the low-frequency noise. However, the intensive use of decap requires extra on-chip area, increases the cost, and becomes impractical if large capacitance values are needed. Runtime control voltage and rollback also can be effective in reducing software errors caused by unstable power supply but with significant performance overheads. Power pad allocation optimization and switchable power-I/O pins are emerging techniques to reduce power pad usage but power supply-I/O bandwidth contention still exists. The situation becomes worse when shifting to 3D-IC for two reasons: 1) the requirements of both I/O bandwidth and power supply increase while the 2D C4 interface for power and I/O connections remains unchanged 2) the cross-layer power supply with through silicon via (TSV) increases wirelength of power supply resulting in a higher impedance of PDN.

In addition to the remaining issues of power delivery and power-I/O contention, the traditional vertical power supply scheme and the horizontal liquid cooling scheme show conflicts. The vertical power supply prefers a thin dielectric layer for cross-layer signal isolation; while inter-layer liquid cooling needs more space for liquid flow, which significantly increases the wirelength of PDN and makes the voltage supply noise severe.

1.6 MultiSpot – a combined thermal and power delivery research infrastructure

The research community has typically tackled thermal and power delivery separately, with different types of tools and different types of solutions. The MultiSpot infrastructure recognizes that the volumetric vs. areal mismatch in 3D-IC applies to both sides of the energy cycle (power in/heat out), which represents a double challenge, but also offers the potential for coordinated solutions. We have previously developed several high-impact architecture modeling tools for power and thermals, such as HotSpot [1], HotLeakage VoltSpot [2], and ArchScope that have enabled extensive research at academic institutions and industry in the areas of temperature-aware computing and pre-RTL power delivery optimization. While the described microchannel enhancement and circuit aspects are essential, breaking the 3D-IC power wall will be suboptimal if the other abstraction levels are not fully engaged. The technological details of the liquid metal fluid or of the embedded capacitor technology are essential for overall system optimization, while the

architecture details of how compute cores are distributed in the stack and how the compute threads are scheduled determine the imbalances in current consumption.

2 3D-IC, microchannel cooling, electronic blood, thermal modeling, power delivery

Our work bridges thermal and power delivery with 3D-IC integration, microchannel cooling and voltage stacking by proposing several unique and combined solutions that enhance the microchannel cooling structure with the capability of power delivery and/or energy storage for heterogeneous systems.

One project that is the most similar to some aspects of this work is the "electronic blood" project pursued by IBM Zurich [3]. The motivation is also the volumetric vs. areal mismatch, and the biology inspiration is taken to the extreme: the electronic blood proposed by IBM both cools the system, but also provides power/energy by using a polarized fluid that can be "charged" off-chip and the charge used on-chip by coupling with the micro-channel that carries the "blood." While this is quite revolutionary, it also happens to be quite impractical as the amount of energy that can be transferred this way is very limited, and the "charging" and "discharging" of the polarized fluid is inefficient. The solution proposed in our work is still to align the power delivery solution to the microchannel cooling, but in a practical way: the energy is delivered still in the form of a current like in the traditional case, except that the current is carried either by the microchannel walls, or by a conductive fluid (liquid metal). The idea of using the microchannel walls as supercapacitors is completely novel as far as we know.

In terms of pre-RTL thermal modeling, our own tool HotSpot is one of the more popular in the research community, and it has also been enhanced with 3D-IC extensions. 3D-ICE from EPFL [4] was specifically developed to model microchannel cooling, but it has many limitations when trying to use it in a architecture-level design space exploration scenario (e.g. is not directly compatible with the set of architecture tools used in the community, such as GEM5, McPAT, etc.). Another limitation of current thermal modeling tools is that they mostly consider homogeneous systems. For power delivery pre-RTL modeling there have been several solutions previously proposed, with our own VoltSpot producing the most detailed spatial and temporal on-chip traces. MultiSpot significantly pushes the envelope in thermal and power delivery modeling by allowing cross-layer coupled analyses while enabling the design space exploration of heterogeneous SoC and SoP systems.

3 Fundamental yet practical solutions for 3D-IC

In this work we are targeting to improve the PDN of 3D-ICs, minimize the power-I/O contention and exploit the design trade-offs between liquid cooling and power delivery. We propose fundamental changes to the power delivery system for 3D-IC and bring out major methodologies of power delivery - liquid cooling co-design for 3D processors and memory (some of the methods are mutually exclusive as they are more appropriate in specific scenarios): 1) reuse microchannels to build voltage noise reduction components – supercapacitors on walls, 2) 3D hierarchical power delivery for 3D-IC and spatially overlap power delivery and liquid cooling – conductive microchannel walls, and 3) physically merge liquid cooling system and power delivery system – liquid metal for cooling and power delivery. Our goal is to seek co-design opportunities of liquid cooling and power delivery to mitigate three major issues for 3D ICs: 1) power delivery instability, 2) power–I/O connections contention, and 3) design conflicts of liquid cooling – power supply.

3.1 Large decoupling capacitors in cooling layer

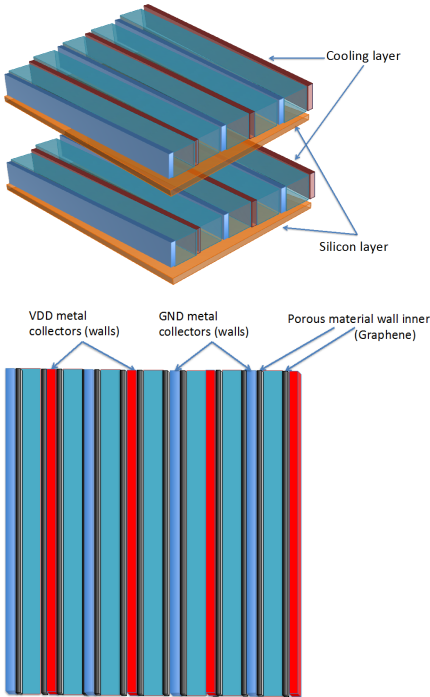
To increase the amount of decap for better voltage noise suppression, we propose an approach to construct supercapacitors by using the structure of the liquid cooling micro-channels. The supercapacitors, based on the electrochemical phenomena of electric double-layer, can provide very high capacitive density, usually 10 to 100 times more energy per unit volume or mass than traditional electrolytic capacitors. However, the supercapacitors need a liquid-solid interface. We therefore propose to utilize the liquid-solid interface of the microchannel to create the electric double layers of supercapacitor. The double-functionality microchannels are therefore called cooling-capacitive microchannel (CCM). To evaluate the benefits of area, cooling and noise reduction when using the CCM, an architectural level chemical physics-electric simulation tool is needed that will extend our existing HotSpot tool and will be integrated in MultiSpot. The real-world benchmark programs will be tested based on this new cooling-power delivery structure. We also propose an approach to partition the micro-channel into multiple short segments to create distributed decaps instead of centralized large decaps. Based on the CCM we construct, we will also build high-efficiency on-chip voltage regulators (VR-CCM). The PDN with VR-CCM will be evaluated against real-world benchmarks.

A supercapacitor has three important components: current collectors, porous electrodes and electrolyte solution. To reuse the structure of liquid-cooling microchannel, we need to consider the double functionality CCM for both heat transfer and electric capacitance. We propose to use the two opposite walls of a cooling microchannel as the current collectors for anode and cathode of a supercapacitor respectively. This structure (Fig. 1) will not lead to the interaction between functions of cooling and electric capacitor for two reasons: 1) the coolant flows along the microchannel while the electric field is imposed perpendicularly to the microchannel walls 2) the heat transfer has much larger time constant than that of the response time of an electric capacitor. The material of the CCM walls should have the properties of high thermal conductivity, high electric conductivity and tensile strength at the same time. The metal materials, such as aluminum, iron and copper are the natural choices which work for both

cooling and electric conductivity. The electrode material needs to be a porous material having high specific surface area, high thermal conductivity, high electric conductivity. High specific surface area porous material means rough surfaces in two opposite walls of microchannel. Previous studies showed the improved liquid-solid heat conductivity caused by rough surface.

Fig. 1 Structure of proposed enhanced microchannel supercapacitor (top view, top, side view, bottom)

Carbon-based materials including activated carbon, carbon nanotubes, carbon nanofibers, carbon onions and graphene are desirable materials for pure electric-double-layer



capacitor. While transition-metal based materials and polymer-based materials may activate the electrochemical pseudocapacitance of the supercapacitor but sacrifice the thermal conductivity a bit.

The electrolyte system needs to have both high specific heat capacity and be suitable for supercapacitors. Aqueous electrolyte, organic electrolyte and ionic liquid are three well-studied electrolyte systems for supercapacitors. The aqueous electrolytes are solutions containing solvent water and salt ions; pure water is the most common coolant of liquid-cooling microchannels. The previous studies show an improved liquid-soild heat tranfer by adding salts to water to create aqueous electrolyte system.

The dynamic behavior of supercapacitors is slightly different from commonly used linear dielectric capacitors. We are building a more accurate equivalent circuit of supercapacitors by considering the nonlinear behavior to study the effectiveness of voltage noise reduction when using supercapacitors. The equivalent circuit of a supercapacitor can be used to enhance the PDN simulator VoltSpot and become part of the MultiSpot tool.

To evaluate the proposed CCM, we are working on a thermal-electric simulator to investigate the effects of cooling and voltage noise reduction. The thermal part is being enhanced to incorporate the ability of simulating liquid-cooling microchannels for 3D IC as part of MultiSpot. The accuracy of the proposed thermal-electric simulator is being validated against a commercial multi-physics simulator.

3.2 Temporal energy storage for power-I/O pin switching using CCM

The switchable power-I/O pin is an emerging technology which switches a subset of the I/O pins to power pins in power-hungry phases of the program, and vice-versa, based on the opposite trends of power-hungry phases and I/O-hungry phases. However, in many scenarios, the power-hungry phases and I/O hungry phases overlap each other, therefore the program has to be slowed down due to either power bottleneck or I/O bottleneck. We plan to utilize the supercapacitor of CCM to power up the processor temporally with limited power supply to shift overlap of power-hungry and I/O-hungry phases.

3.3 Hierarchical 3D power delivery via cooling layer

To minimize the contention between power delivery and I/O connections, we propose a 3D hierarchical power delivery network design. This design joins the power delivery and liquid cooling systems and leads to more compact and efficient cooling-power co-design. We propose two separate schemes: one to insert metal wires in the intermediate space between the cooling layers, another one directly adopts the conductive walls of the CCM as wires. In each scheme, for each cooling layer, we propose to have one or several power redistribution layers to connect to the corresponding silicon layer. And one or more vertical coarse-granularity power distribution layers are built vertically to connect the power from PCB board to the in-cooling-layer power wires. The proposed 3D hierarchical PDN is being evaluated and benchmarked against traditional 2D power delivery designs with real-world benchmark programs.

3.4 Horizontal power delivery via cooling layer

The liquid-cooling microchannels need to be placed in parallel to the silicon die to maximize the heat transfer interface area, while the traditional PDN of 3D ICs distribute current laterally in package through C4 pads and then spread vertically within multi-layers via TSVs. As a natural sequence, the lateral microchannels and vertical TSVs can easily block each other. The spatial connection between microchannels and TSVs causes high design complexity and lowers down the cooling effect and the total number of TSV (both power TSV and I/O TSV). We propose a hierarchical 4-level 3D power delivery topology. Herein, a PDN of the proposed topology partially spreads power laterally in package level with fat metal layers, then redistributes vertically with fat metal layers vertically, and then spreads laterally along the direction of microchannels in the cooling layer with fine metal, finally redistributes to

silicon layers with very fine metal layers. This topology minimizes the number and occupied area of the vertical cross-layer power TSVs and therefore reduces the spatial conflict between lateral cooling microchannel and vertical TSVs and contention between power TSV and I/O TSVs.

3.5 Cooling-power-capacitive microchannel

Combining the idea of hierarchical 3D power delivery and cooling-capacitive microchannel (CCM), we propose to use the walls (collectors) of CCM as lateral power distribution wires, called cooling-power-capacitive microchannel (CPCM). This design further reduces the spatial contention between power delivery and cooling to allow more microchannels. In addition, by incorporating the capacitance of CCM to the hierarchical 3D power delivery, further voltage noise reduction is expected.

3.6 Cooling-power microchannel

Finally, as another method for dual use microchannels we propose to use high-conductivity, liquid metal, as the coolant for the liquid cooling system; therefore the micro-channels are capable of both cooling and power delivery.

The cooling-power-capacitive microchannel utilize the walls of microchannels for power delivery. We propose an alternative design which utilizes both the liquid and the walls of microchannel for power delivery, called cooling-power microchannel (CPM). The CPM design simply merges the liquid cooling system and the power distribution networks into one joint system and therefore makes the joint system more compact than the previous schemes. Electrolyte solution cannot provide enough conductivity to delivery power, therefore we switch to high electric-conductive liquid material – liquid metal. Because power delivery needs two isolated networks for VDD and GND, we consider two separate but equivalent cooling-power subsystems for VDD and GND respectively. As a competitive design, the CPM will compare with the CPCM.

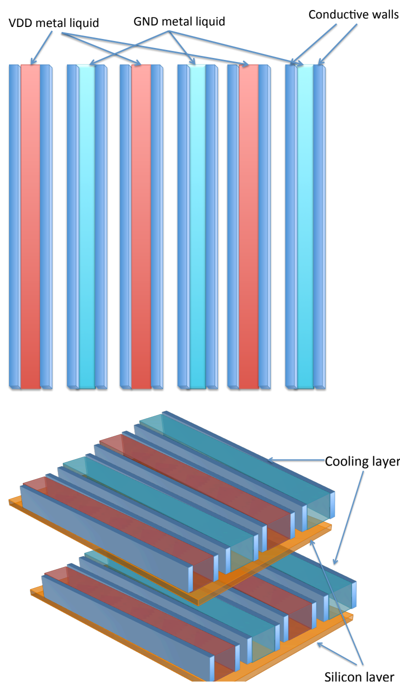


Fig. 2 Structure of proposed enhanced microchannel liquid metal (top view, top, side view, bottom)

3.7 Liquid-cooling-power delivery co-designs for 3D memory architectures

Micron's hybrid memory cube (HMC) is the first commercial 3D IC device which provides more than 15X the performance, 70% less energy than traditional DDR3 technologies and 90% less space than today's RDIMMs. However the number of silicon layers is limited by power delivery and thermal constraints. Since the HMC is a 3D memory architecture, more I/O bandwidth but less power supply than those of processors are required. We intend to evaluate the proposed cooling-power co-design techniques: cooling-capacitive microchannel, cooling-power-capacitive microchannel and cooling-power microchannel to the HMC. New trade-offs between I/O, power supply and cooling will be studied to better utilize the proposed cooling-power co-design schemes.

4 Preliminary Results

For the enhanced microchannel work we have tried to derive some first order estimations of the expected improvements which show that indeed these ideas can provide tremendous benefits that enable future 3D-IC development.

4.1 Microchannel supercap for use during brownouts or to provide extra power during boost

According to [5], the electrodes are 230µm in width, 10mm in length, 200µm interspace and 0.312µm thinkness, which leads to 11.074µF/mm^2. Think about a cooling channel 230µm in width and 31.2µm in height. The capacitive channel design lead to 1.1074mF/mm^2. Given the reference 3D IC system described in [Zha15b], the chip has an area of 44.12 mm^2 which leads to 48.858mF per cooling layer. Given the case of 10% frequency boost, we have 9.20W per each silicon layer (7.6W on 1GHz). The extra power needed is 1.60W. The theoretical extra energy can provided by supercap is $½*[2.7^2-1.1^2)*48.858$mF = 0.14853J which can support 1.60W extra power for about 93ms.

4.2 Microchannel using liquid metal for cooling and power delivery

According to [6], Gallium is the best candidate of liquid metal cooling, whose thermal capacity and viscosity are very close to those of water by much better thermal conductivity. We assume a 3D-IC system but replace the coolant with Gallium. The total area of fluidic via is 1mm^2 (1% die area). The total length is 150µm given die thickness is 50µm. The total resistance is 40.5µOhm. While if use power TSV, [7] shows (240.4mV-118.8mV)/100A = 1.216mOhm; thus the liquid metal cooling strategy cut the power delivery resistance to 1/3 of the power TSV solution. Since Gallium is highly corrosive it imposes constraints on the appropriate electrical contacts to the PDN, luckily

Tungsten, already a common metal used in IC fabrication can serve this role.

4.3 PDN and Thermal modeling

Our prior work on HotSpot and VoltSpot has served the research community well, yet there are also many aspects that MultiSpot enhances: the possibility of PDN/thermal codesign, extensions for heterogeneous systems, multiple cooling methods including microchannel cooling, multiple power delivery solutions, including CCM, multiple decap solutions including supercapacitors, etc.

4.4 Architecture level modeling of power delivery and heat removal for 3D-IC

In order to fully take advantage of the proposed solutions we need to take into account the implications at the architecture and system levels. We already have extensive experience with cross-layer issues from our work on the HotSpot thermal modeling tool and VoltSpot power delivery tool that include physical and circuit level considerations in an architecture modeling infrastructure. For the MultiSpot project we include 3D-IC aspects, including enhanced microchannel cooling and voltage stacking into a computer architecture infrastructure that will include GEM5 for functional simulation, McPAT for power modeling, and our MultiSpot for power delivery and thermal modeling. In order to reflect the 3D-IC details GEM5 is being augmented with a 3D-NOC and a 3D mesh many-core topology that will map NOC routers and processor cores according to the 3D-IC stack, McPAT is being enhanced by adding fluid power, voltage stacking and explicit switched-capacitor regulator details in the power number calculations, VoltSpot is being enhanced by the addition of conductive microchannels, supercapacitor structures, TSVs and switched-capacitor regulation, while HotSpot, enhanced with 3D-IC microchannel cooling, is being used for self-consistent power and thermal simulations for a heterogeneous SoC or SoP.

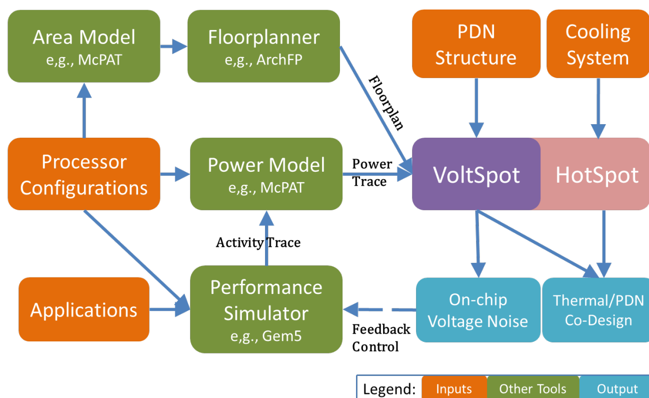


Fig. 3 Current architecture tools for thermal/PDN. Multispot enhances and replaces VoltSpot/HotSpot

5 Conclusions and future work

The described methods can have a significant impact on the semiconductor industry and on society as a whole. By breaking the power wall for 3D-IC, thus providing a practical path forward for Moore's law, future electronic systems can continue to become smaller, less costly, with higher functionality and with longer lasting batteries. As with our previous tools we plan to release MultiSpot for wide usage by the research community.

Acknowledgements

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