A Survey on ARM Cortex A Processors

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Overview of ARM Processors

- Focusing on Cortex A9 & Cortex A15
- ARM ships no processors but only IP cores
  - For SoC integration
- Targeting markets:
  - Netbooks, tablets, smart phones, game console
  - Digital Home Entertainment
  - Home and Web 2.0 Servers
  - Wireless Infrastructure
- Design Goals
  - Performance, Power, Easy Synthesis
ARM Cortex A9/A15

- 1-4 Cores
- Out-of-Order Superscalar
- Branch predictor
- 32KB L1 I/D caches
- ~4MB L2 caches with Coherency
- NEON(SIMD) & FPU
- 32/28nm (A15) 45nm (A9)
Texas Instrument OMAP5

TI OMAP5430 SoC

LMDDR2 LPDDR2 NAND/NOR Flash SD eMMC SSD USB SS/HS host/target

OMAP5430

Dynamic memory manager L2 cache ARM Cortex-M4 ARM Cortex-M4

ARM Cortex-A15 MPCore (up to 2 GHz) POWERVR SGX544-MPx 3D graphics

ARM Cortex-A15 MPCore (up to 2 GHz) TI 20 graphics IVA-HD video processor

L3 Network-on-chip interconnect

Timers, int Controller, Mailboxes, System DMA Audio processor

Boot/Secure ROM, L3 RAM M-Shield™ system security technology: SHA-1/SHA-2/MD5, DES/3DES, RNG, AES, PKA, secure WDT, keys, crypto DMA

L4 peripherals Multi-pipe display sub-system (DSS)

Multi-pipe display sub-system (DSS)

Debug & trace UART GPIO Keypad PC/SPI

Trace analyzer GPIO Keypad Touch screen controller

Emulator pod Touch screen controller

Fast IrDA HDMI 1.4a

UPD125015 3D HDTV

HDQ/I-Wire REF/CLK (4) UARTs

Main battery Power Monitor

3G/4G modem WiLink™ wireless connectivity

2x MIPI® HSI MIPI LLI TI C2C USB/HSC/C UART/SPI SDIO McBSP PC/SPI SDIO UART McBSP

TP04100 Audio

Headset Speakers Vibrators Amplifiers Micro

TWL6040

32 kHz Crystal In/Out

HF speakers Handset microphone

Up to four displays

Up to four cameras

Camera control DIG MIC

PDM SLIMbus®
# Comparison of ARM, Atom, i7

<table>
<thead>
<tr>
<th></th>
<th>Cortex A15 (no L2, 32nm)</th>
<th>Cortex A9 (no L2, 40nm)</th>
<th>Atom N270 (45nm)</th>
<th>I7 960 (45nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Cores</td>
<td>2 (4 maximum)</td>
<td>2 (4 maximum)</td>
<td>1 Core, 2 HT threads</td>
<td>4 Cores, 8 HT threads</td>
</tr>
<tr>
<td>Frequency</td>
<td>1Ghz – 2.5 Ghz</td>
<td>800Mhz (Po) 2Ghz (Per)</td>
<td>1.6 Ghz</td>
<td>3.2 Ghz</td>
</tr>
<tr>
<td>Out-of-Order?</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>L1 cache size</td>
<td>32KB I/D</td>
<td>32KB I/D</td>
<td>32KB I/D</td>
<td>32KB I/D</td>
</tr>
<tr>
<td>L2 cache size</td>
<td>N/A</td>
<td>N/A</td>
<td>512KB</td>
<td>1MB + 8MB L3</td>
</tr>
<tr>
<td>Issue Width</td>
<td>4</td>
<td>4</td>
<td>2</td>
<td>4?</td>
</tr>
<tr>
<td>Pipeline Stages</td>
<td>?</td>
<td>8</td>
<td>16</td>
<td>14 ~ 24 (?)</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>?</td>
<td>1.05V (Per)</td>
<td>0.9 – 1.1625 V</td>
<td>0.8-1.375 V</td>
</tr>
<tr>
<td>Transistor Count</td>
<td>?</td>
<td>26,00,000?</td>
<td>47,000,000</td>
<td>731,000,000</td>
</tr>
<tr>
<td>Die size</td>
<td>?</td>
<td>4.6 mm2 (Po) 6.7 mm2 (Per)</td>
<td>26 mm2</td>
<td>263 mm2</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>?</td>
<td>0.5 W (Po) 1.9 W (Per)</td>
<td>2.5W (TDP)</td>
<td>130W (TDP)</td>
</tr>
</tbody>
</table>
## Comparison of ARM SoC, Atom, i7

<table>
<thead>
<tr>
<th></th>
<th>TI OMAP5 (28nm)</th>
<th>Nvidia Tegra 2 (40nm)</th>
<th>Atom N450 (45nm)</th>
<th>I7 2600S (32nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CPU Cores</strong></td>
<td>2 x A15</td>
<td>2 x A9</td>
<td>1 Core, 2 HT threads</td>
<td>4 Cores, 8 HT threads</td>
</tr>
<tr>
<td><strong>CPU Freq.</strong></td>
<td>2Ghz (A15)</td>
<td>1Ghz</td>
<td>1.66Ghz</td>
<td>2.6Ghz</td>
</tr>
<tr>
<td><strong>GPUs ASICs</strong></td>
<td>Video, Audio, Encryption, Display, 2D/3D</td>
<td>8x GPUs, Audio, Video, ISP</td>
<td>1 GPU</td>
<td>1 GPU</td>
</tr>
<tr>
<td><strong>L2</strong></td>
<td>?</td>
<td>1MB</td>
<td>512KB</td>
<td>1MB+8MB</td>
</tr>
<tr>
<td><strong>Die Size</strong></td>
<td>?</td>
<td>49mm2</td>
<td>66mm2</td>
<td>?</td>
</tr>
<tr>
<td><strong>Transistors</strong></td>
<td>?</td>
<td>260,000,000</td>
<td>123,000,000</td>
<td>?</td>
</tr>
<tr>
<td><strong>Package Size</strong></td>
<td>17 x 17 mm2</td>
<td>23 x 23 mm2</td>
<td>22 x 22 mm2</td>
<td>37.5 x 37.5 mm2</td>
</tr>
<tr>
<td><strong>Power Consumption</strong></td>
<td>?</td>
<td>150~500mW ?</td>
<td>5.5W (TDP)</td>
<td>65W (TDP)</td>
</tr>
</tbody>
</table>
Power/Performance Optimization as a SoC

- Application-specific SoC design
  - Integrate different ASICs
  - Customize Cortex Processors
  - Reduced memory bandwidth & frequency
- Mixing High Vt / Low Vt transistors
- Twisting floorplan, routing, clock tree design
- Power gating/Clock gating/DVFS
  - Four modes: Run, Standby, Dormant, Shutdown
  - Fine-grained pipeline shutdown
  - Faster register save and restore (state save/restore)
  - Power domains & voltage domains
Power Saving as SoC: Power Gating

- Different power domains
  - Cores
  - NEON/VFP
  - Debug Interface
  - L2 cache tags (per bank)
  - L2 cache control
  - Interrupt Controllers

- Impact of power gating
  - 3% reduction in performance
  - 2% increase in area
  - 4% increase in dynamic power
  - 95% decrease in power when turned off
Power/Performance as a CPU

- Performance Enhancement (power hungry techniques)
  - Dynamic issue design
  - 4-way superscalar
  - Complex Branch predictor
  - Large L1/L2 caches

- Power savings
  - Accurate branch prediction
  - Micro TLB
  - RISC
  - SIMD, Jazzelle RCT etc.
ARM Instruction Set Architecture

• ARM processor architecture supports 32-bit ARM and 16-bit Thumb ISAs

• ARM architecture -- RISC architecture
  ➢ Large uniform register file
  ➢ Load/store architecture
  ➢ Simple addressing modes
  ➢ Auto-increment and auto-decrement addressing modes
  ➢ Load and Store multiple instructions

• Instructions can also be "conditionalised" based on condition code in Application Program Status Register
ARM Instruction Set Architecture

• Thumb
  ➢ Extension to the 32-bit ARM architecture
  ➢ Features a subset of the most commonly used 32-bit ARM instructions compressed into 16-bit opcodes
  ➢ Excellent code-density for minimal system memory size, reduced cost and power efficiency
  ➢ Designers have the flexibility to emphasize performance or code size
  ➢ "Thumb-aware" core is a standard ARM processor fitted with a Thumb decompressor in the instruction pipeline

• ARM uses the Universal Assembly Language
DSP

• ISA extension

• Features: new instructions to load and store pairs of registers, 2-3 x DSP performance improvement over ARM7

• Eliminates the need for additional hardware accelerators

• Provides high performance solution with low power consumption

• Reuses existing OS and application code

• Supports including servo motor control, Voice over IP (VOIP) and video & audio codecs
SIMD

• 75% higher performance for multimedia processing in embedded devices
• “Near zero" increase in power consumption
• Simultaneous computation of 2x16-bit or 4x8-bit operands
• Offers single tool-chain and processing device, transparent of OS
NEON

• Cleanly architected and works seamlessly with its own independent pipeline and register file

• Large NEON register file with its dual 128-bit/64-bit views enables efficient handling of data
  ➢ Minimizes access to memory, enhancing data throughput

• Designed for autovectorizing compilers and hand coding

• Provides flexible and powerful acceleration for consumer multimedia applications
  ➢ Supports the widest range of multimedia codecs used for internet applications
NEON
Vector Floating Point Architecture

• Coprocessor extension to the ARM architecture

• Supports floating point operations in half-, single- and double-precision floating point arithmetic

• Fully IEEE 754 compliant with full software library support

• Supports execution of short vector instructions but these operate on each vector element sequentially

• Three-dimensional graphics and digital audio, printers, set-top boxes, and automotive applications
Jazzelle

- Combined hardware and software solution for accelerating execution
- Software -- fully featured multi-tasking JVM
- Hardware -- coprocessor CP14 provides support for the hardware acceleration
- Jazzelle DBX technology for direct bytecode execution – Direct interpretation bytecode to machine code
- Jazzelle RCT technology supports efficient AOT and JIT compilation with and beyond Java
Jazzelle

- Jazelle DBX and RCT are cache and memory efficient, maintaining low power
- Jazelle DBX is a robust and proven solution and easy to integrate
- Jazelle RCT provides an excellent target for any runtime compilation technology

Developers’ Flexibility
- Resource constraint device: Jazelle DBX only
- On high-end platforms, Jazelle RCT alone with JIT and AOT
Conclusion

- Aggressive power hungry design targeting at high single thread performance
  - Out-of-Order Execution
  - Wide superscalar
  - Large caches with coherency protocols
- Power saving techniques for ARM CPUs
  - RISC
  - ISA Optimization: Thumb, Thumb2, ThumbEE
  - Application-Specific Components: SIMD, DSP, VFPUs, Jazzelle
- Power saving techniques for SoC chips
  - Fine-grained power gating & clock gating & DVFS
  - Fine-grained pipeline shutdown
  - Fast registers saving/restoring
  - Customizable CPU components
  - Mixing high Vt and low Vt transistors
Reading materials

- Keys to Silicon Realization of Gigahertz Performance and Low Power ARM Cortex-A15, Lamber A. et. al., ARM Technology Conference 2010