

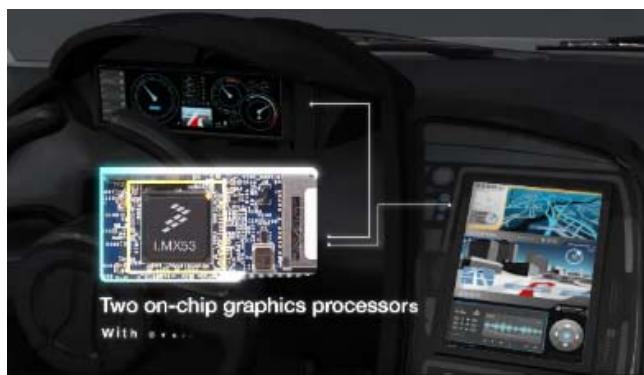
Freescale i. MX

Shuai Che

Feb 15, 2011

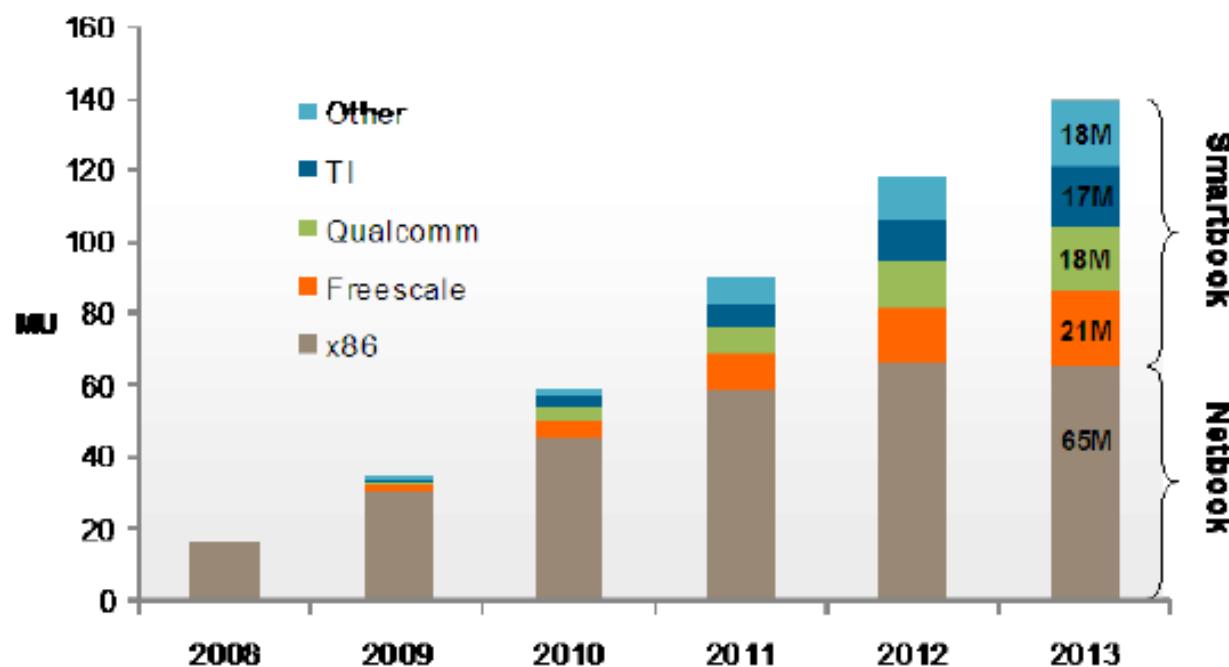
i. MX Market Segmentation

- Automotive
- Smart Mobile Devices (e.g. tablets, smartbooks)
- eReaders
- Embedded Multimedia



Freescale Market Share

- Pioneer in portable media player (PMP) market and eBook application processors



Source: ABI Research April 2009

Example of
Consumer usage:

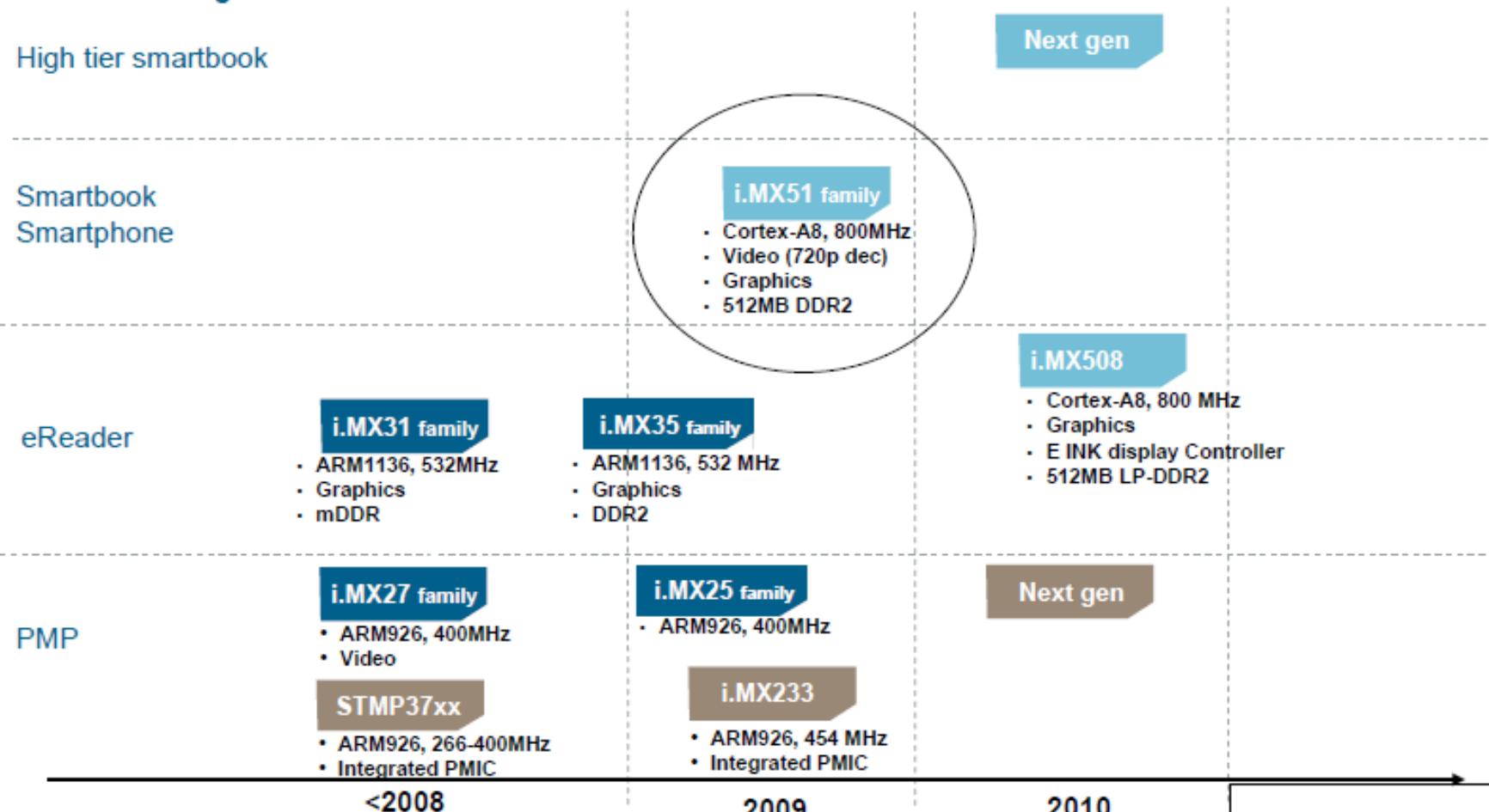
High tier smartbook

Smartbook
Smartphone

eReader

PMP

Applications Processors (i.MX) Roadmap



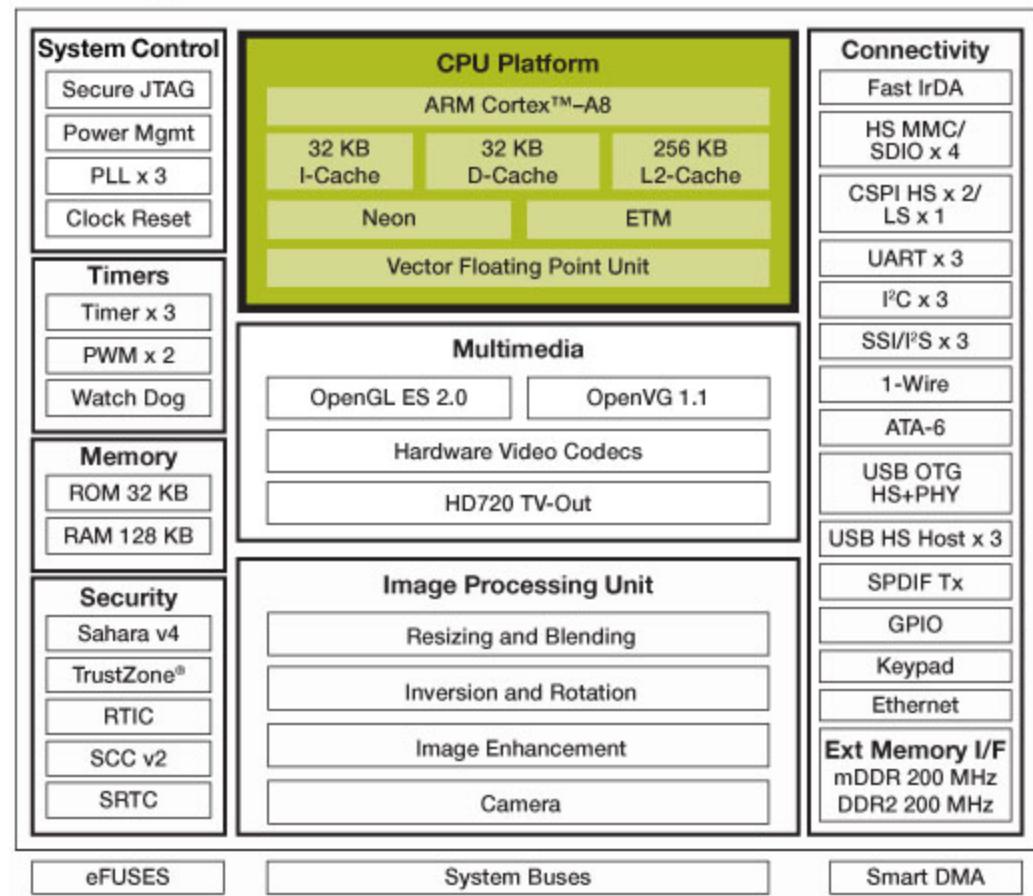
Right Edge = Consumer Qualification

Left Edge has no meaning

Freescale, the Freescale logo, AllVec, C-S, CodeTEST, CodeWarrior, ColdFire, C-Ware, mobileGT, PowerQUICC, StarCore, and Symphony are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. BeeKit, BeeStack, ConNet, the Energy Efficient Solutions logo, Flexis, MXC, Platform in a Package, Processor Expert, QorIQ, QUICC Engine, SMARTMOS, TurboLink and VirtIQo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. © 2010 Freescale Semiconductor, Inc.

i.MX 515

- Smartphones/smartbooks, navigation devices, PMP and PDAs, etc.
- CPU
 - 800 MHz ARM Cortex-A8 CPU
 - 32KB instruction and data caches
 - Unified 256KB L2 cache
 - NEON SIMD media accelerator
 - Vector floating point co-processor
- Multimedia
 - 2D/3D graphics
 - Video processing units
- Image processing unit
 - Image rotation, resizing, etc.
 - Two camera sensor ports
- Security support
 - AES, DES, MD5, SHA ...
- 65nm process, 19x19 package





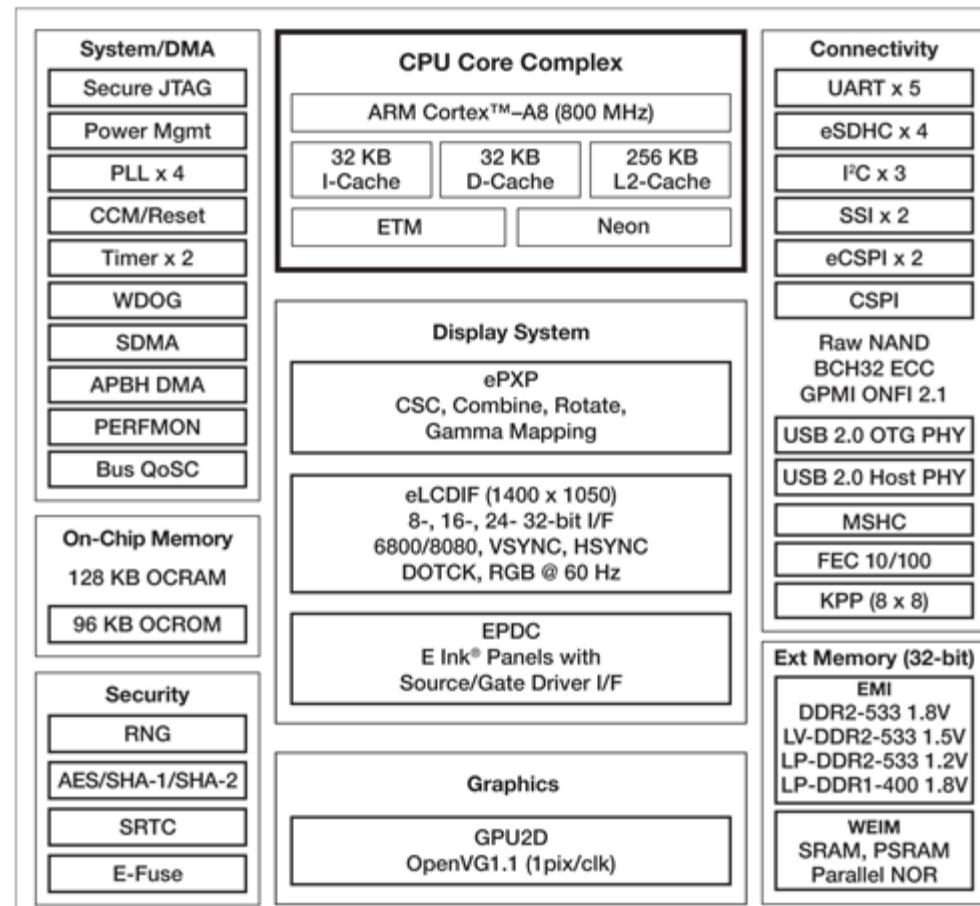
i. MX508 for eReader

- The Kindle 2 uses a *Freescale* 532 MHz, ARM-11 processor
- The Kindle 3 uses a *Freescale* i. MX353 application processor
- Both use Epson e-paper display (EPD) controller
- E Ink is the leading panel solution
- Freescale: 70-90% of market share in 2009



i. MX 508

- Designed for E-readers
- CPU
 - 800 MHz ARM Cortex-A8 CPU
 - 32KB instruction and data caches
 - Unified 256KB L2 cache
 - NEON SIMD media accelerator
 - Vector floating point co-processor
- **Integrated** E-INK EPD controller
- ePXP: color space conversion, rotation and scaling, etc
- An integrated NEON DSP and 2-D graphics accelerator for PDF, Adobe Flash, etc.

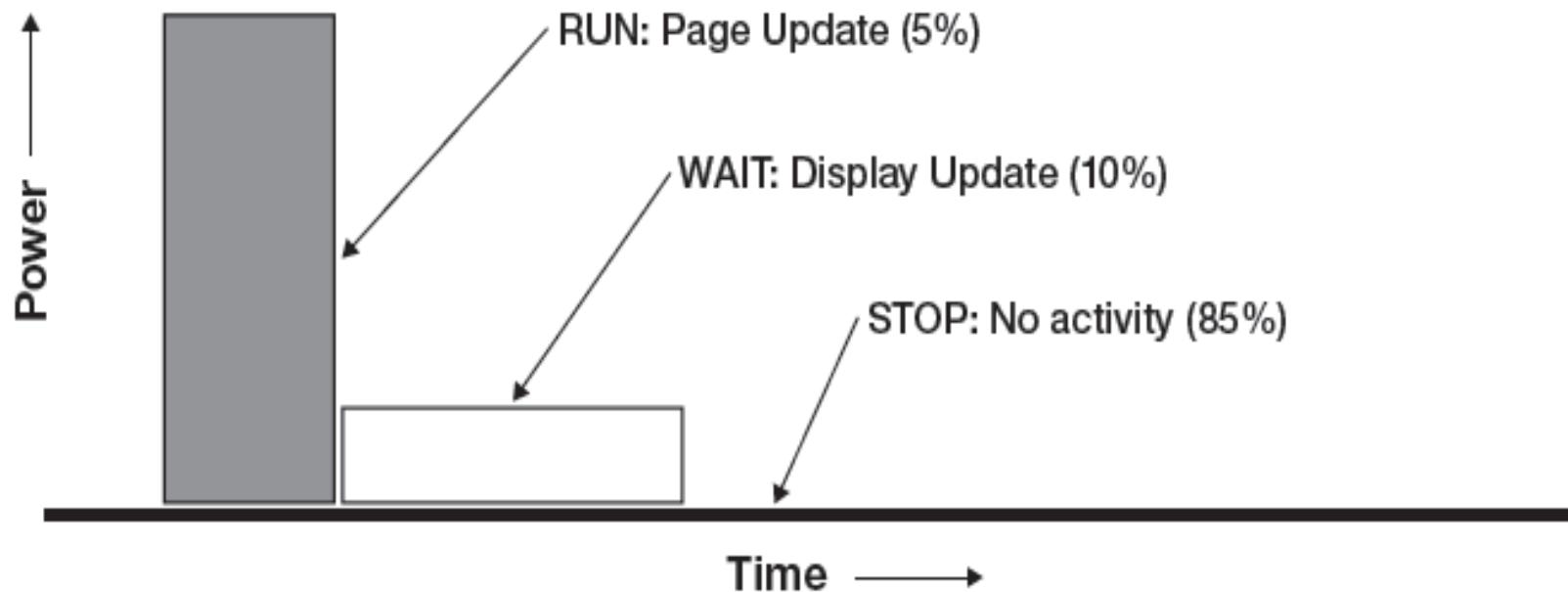


Benchmark Results

PDF file benchmark on ARM cores (time to open a pdf file):

	pdf file 1 65 pages of text 243KB	pdf file 2 4 color pages (ads) 731KB	pdf file 3 EDN magazine 66 pages (ads, text) 16500KB
Cortex A8 i.MX51 800MHz DDR2 200MHz	< 1 sec	~2 sec	~6 sec
Cortex A8 i.MX51 532MHz DDR2 133MHz	~1 sec	~4 sec	~8 sec
ARM11 i.MX35 532MHz DDR2 133MHz	~1.5 sec	~6 sec	~15 sec
ARM9 i.MX25 400MHz DDR2 133MHz	~2 sec	~10 sec	~25 sec

A Typical Scenario for eReader



Power Saving Strategy for eReader

- A powerful CPU for fast file processing
- Low-power transistors in the peripherals and high performance transistors in the CPU
- Independent power domains
- Dynamic voltage and frequency scaling
- A relatively large cache

Power Management Features for i.MX

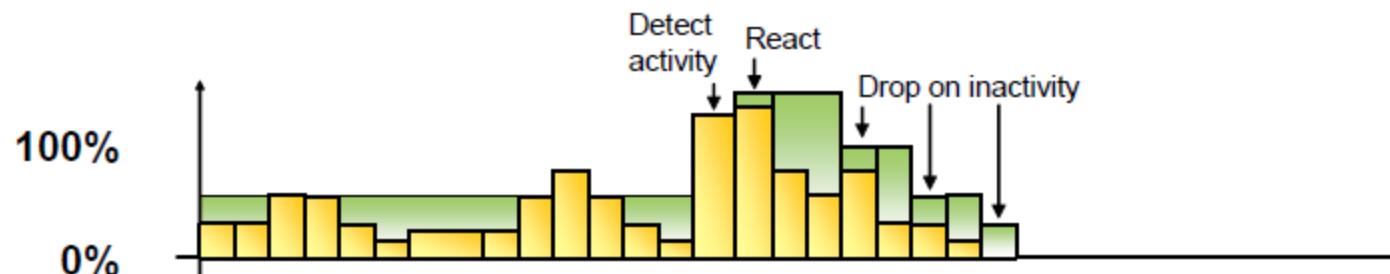
$$Power = \text{Dynamic} + \text{Static}$$

- Dynamic frequency and voltage scaling (DVFS)
- Dynamic Process Temperature Compensation (DPTC)
- Power Gating
- Active Well-Biasing
- Clock Gating
- Low Power Modes

Power Management Features for i.MX

- Dynamic Voltage Frequency Scaling
- Two modes:

Reactive Approach—Hardware Solution



Predictive Approach—Hardware and Software Solution

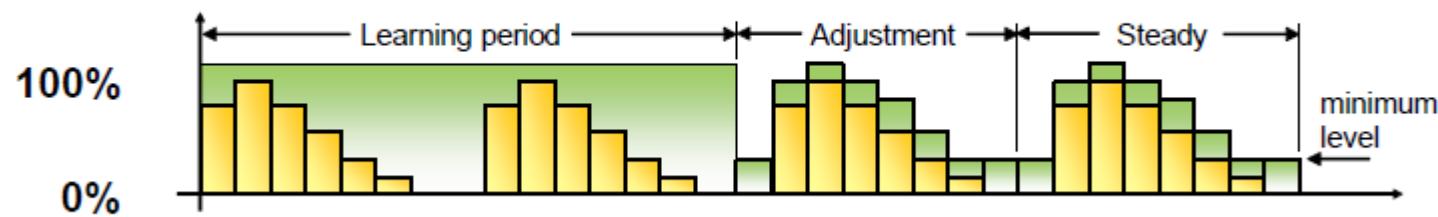


Figure 3. DFVS Approaches

Power Management Features for i.MX

- Dynamic Process Temperature Compensation
 - “*DPTC mechanism measures delays of reference circuits that are dependent on the process speed and temperature, then lowers the voltage to the minimum level needed to support the current operating frequency.*”
- For i. MX 31, under room temperature,
 - 1.6 V for a conventional 90 nm design
 - 1.2 V for DPTC-enabled 90 nm design (40% savings)

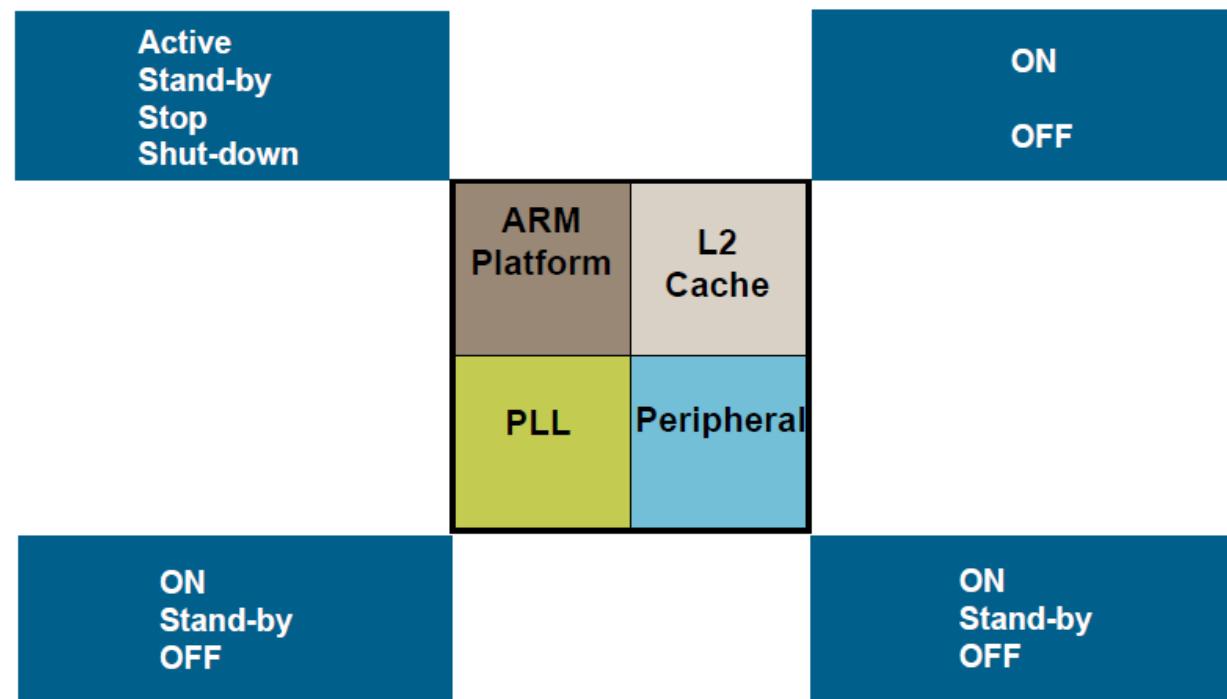
Power Management Features for i.MX

- Power Saving Modes

RUN	Normal operating mode. Core frequency and operating voltage can be dynamically changed within a range.
Wait	MCU clock remains gated. Operation resumes on interrupt.
Doze	MCU and MAX clocks remain gated. Operation resumes on operation. Peripherals not requiring MCU/MAX functionality can remain active. Normal operation resumes on interrupt.
State Retention	MCU and peripheral clocks gated. SDRAM in self-refresh mode. Supply voltage can be dropped to minimum.
Deep Sleep	Clocks gated. ARM platform power supply OFF. Normal operation resumed on interrupt.
Hibernate	All power OFF. System completely dead; operation resume equivalent to cold boot.

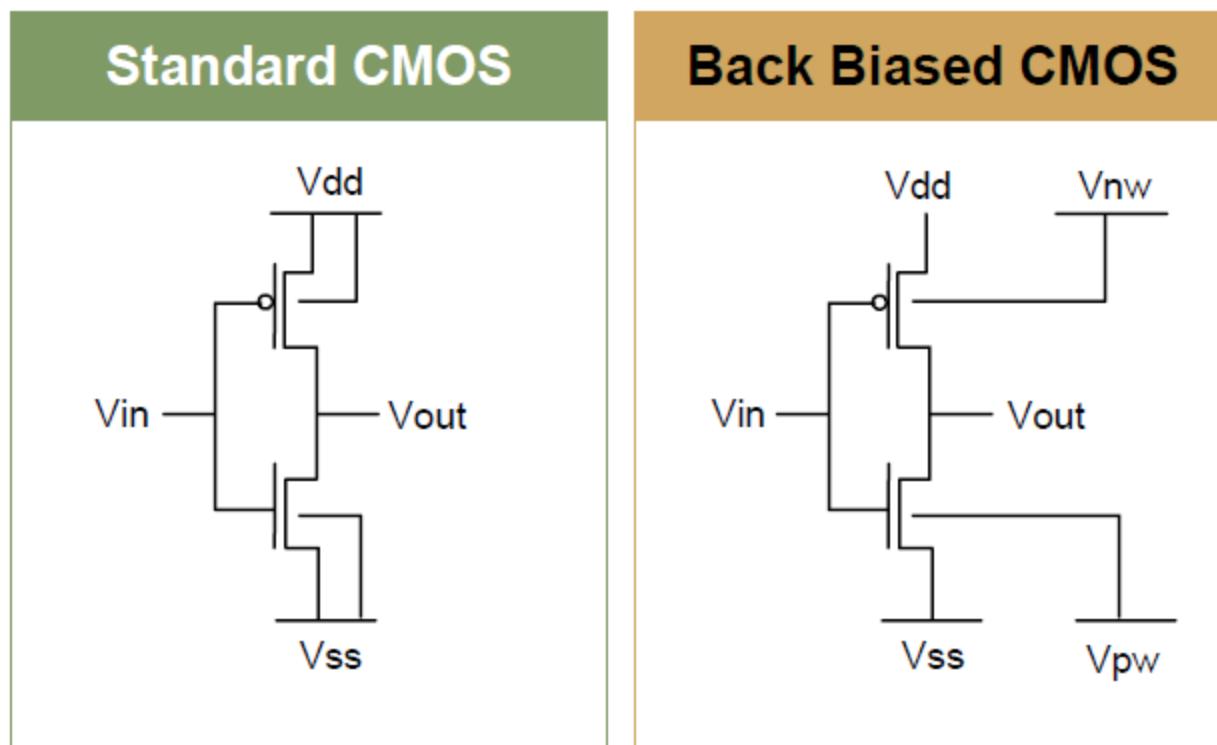
Power Management Features for i.MX

- Power Domains
- Flexibility of clocking-off/powering-off different parts



Power Management Features for i.MX

- Active Well-Bias (AWB)



The New i.MX 6

- i.MX 6
 - Solo/Dual/Qual families based on Cortex A9 Cores
 - 3-D graphics and 1080p encode/decode
 - Tablets, smartbooks, automotive infotainment and eReaders

Thank you!

The eReader ecosystem

