Research Challenges on Temperature-Aware Computer Systems

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Temperature Affects Cooling Cost

- IBM S/390:
  - 350-V bulk power subassembly (under cover)
  - Processor cage:
    - Contains processors, memory and I/O
    - Dual redundant three-phase line cord
    - Distributes power to system
    - Five I/O slots
  - MCM/evaporator
  - 350-V integrated battery
  - Modular cooling unit
  - Expansion cage:
    - Powered from processor cage
    - Twenty-two I/O slots

Temperature Affects Performance and Power

Temperature Affects Reliability

The Arrhenius Equation: \( \text{MTF} = A \exp\left(\frac{E_a}{K \cdot T}\right) \)

- \( \text{MTF} \): mean time to failure at \( T \)
- \( A \): empirical constant
- \( E_a \): activation energy
- \( K \): Boltzmann's constant
- \( T \): absolute temperature

Failure mechanisms
- Die metalization (Corrosion, Electromigration, Contact spiking)
- Oxide (charge trapping, gate oxide breakdown, hot electrons)
- Device (ionic contamination, second breakdown, surface-charge)
- Die attach (fracture, thermal breakdown, adhesion fatigue)
- Interconnect (wirebond failure, flip-chip joint failure)
- Package (cracking, whisker and dendritic growth, lid seal failure)

Most of the above increase with \( T \) (Arrhenius)
Notable exception: hot electrons are worse at low temperatures
Temperature Variation

Temporal variation of SPEC applications over time

Source: “A Quick Thermal Tutorial”
Kevin Skadron, Mircea Stan, U. of Virginia 2005

Spatial

Thermal Map Pentium M (simulated)
(lowest) blue, green, yellow, orange, red (highest)

Source: Lev Finkelstein, Intel 2005

The Thermal Wall

Performance scaling of microprocessors

Same area (Moore’s law)
- Typical growth factors: 1.75X per generation
- Same area: 1.75X per generation
- Same power: 1.55X per generation

In a thermally limited environment
Evolutionary Uarch will diminish its performance return

Source: Ronny Ronen
**Basic Concepts**

- Temperature is a function of power density
- Reducing temperature implies
  - Increasing area
    - Increases wire delays $\rightarrow$ Big impact on performance
  - Reducing power (slower transistors, simpler blocks)
    - May impact performance if not done carefully

**Critical Areas of Research**

- Modeling
  - Heat transfer
  - Thermal sensor’s response
- Floorplan
  - Tradeoff between wire delays and peak temperature
- Microarchitecture techniques
  - Throttling
  - Clustering
    - Thermal steering
    - Cluster hopping
  - DVS/DFS
    - GALS
    - At the core granularity (multi-core)
  - Adaptive microarchitectures
- More effective cooling solutions
  - Constrained by weight, noise and power
**Will Put Off the Thermal Wall but...**

- A breakthrough is needed
  - New materials (e.g. High-K gate dielectric)
  - New devices (e.g. Tri-gate transistors)
  - New technology (e.g. carbon nanotubes, III-V transistors)
  - New circuit design techniques (e.g. asynchronous)
  - New microarchitectures (e.g. many simple cores)
  - ...

**The Challenge:**

*Reduce Energy While Increasing Performance*