

TANIYA SIDDIQUA

AREA OF INTEREST

- Computer Architecture, VLSI Circuit Design

EDUCATION

- **PhD Candidate**, Department of Computer Science, University of Virginia, (2009-present), Cumulative GPA: 3.91/4.00. (Expected Summer, 2012)
Dissertation Topic: A Multi-level Approach to Processor and Memory Reliability
- **MS in Computer Science**, Department of Computer Science, University of Virginia, (2007-2009), Cumulative GPA: 3.90/4.00.
Thesis: Balancing Soft Error Coverage with Lifetime Reliability in Redundantly Multithreaded Processors
- **Bachelor of Science in Computer Science and Engineering**, Department of Computer Science and Engineering, Bangladesh University of Engineering and Technology (BUET), (2000-2005), Cumulative GPA: 3.77/4.00.
Thesis: XML Compression Using Arithmetic Coding

WORK EXPERIENCE

- **Graduate Technical Intern at Intel Corp.** (Summer'2011-Fall'2011):
Technology for Reliable Usage Group
Manager: Arijit Biswas, Mentor: Athanasios E. Papathanasiou
Job Description: Development of a set of error analysis tools, analysis of the processor and DRAM error data to estimate hard and soft error rates and development of a memory error prediction model.
- **Research Assistant at University of Virginia** (Spring'2008-present):
Advisor: Dr. Sudhanva Gurumurthi.
- **Teaching Assistant at University of Virginia** (Fall'2007-Spring'2008):
Courses Taken: E-Commerce Technologies, Advanced Computer Architecture, Introduction to Programming
- **Lecturer**, Department of CSE, BRAC University (Spring'2006-Summer'2007)
Courses Taken: Computer Architecture, Digital System Design, Microprocessors, Digital Logic Design, Artificial Intelligence, Computer Networks, Algorithms, C Programming Language

AWARDS

- **Spontaneous Recognition Award**, Intel, 2011
- **Cyber Physical Systems Summer School Scholarship**, Georgia Institute of Tech, 2010
- **GLSVLSI Travel Grant Award**, 2010
- **1st Place in Student Research Competition**, Grace Hopper Conference, 2009
- **Grace Hopper Scholarship for Hardware Research**, Sun Microsystems, 2009
- **Cash Award, Travel Grant, ACM Student Research Competition**, 2009
- **Travel Grant**, CRA-W Grad Cohort 2009, CRA-W/CDC PLOSA 2009, ISCA 2009
- **Golden Key Intrl. Honor Society's Top 15% Graduate Std Award**, 2008
- **Graduate Teaching Fellowship**, University of Virginia
- **Dean's Merit List Award**, BUET
- **University Merit Scholarship**, awarded to top 10% in a semester, BUET
- **3rd Place and Best Female Team**, The 26th ACM ICPC, Asia Regional 2001
- **Best Student Award, 1997** - S.K.B.Z. Bangladesh Islamia School

PUBLICATIONS

▪ Journal/Refereed Conference/Workshop Papers:

1. T. Siddiqua, S. Gurumurthi, "Enhancing Recovery in SRAM Arrays Through Recovery Boosting", IEEE Transactions on Very Large Scale Integration Systems, 2011.
2. T. Siddiqua, S. Gurumurthi and M.R. Stan, "Modeling and Analyzing NBTI in the Presence of Process Variation", ISQED, March 2011.
3. T. Siddiqua, S. Gurumurthi, "Recovery Boosting: A Technique to Enhance NBTI Recovery in SRAM Arrays", ISVLSI, July 2010. (Acceptance Rate=33%)
4. V. Mohan, T. Siddiqua, S. Gurumurthi, M.R. Stan, "Modeling and Evaluating NAND Flash Endurance in SSDs", 2nd Workshop on Hot Topics in Storage and File Systems (HotStorage), June 2010. (Acceptance Rate=31%)
5. T. Siddiqua, S. Gurumurthi, "A Multi-Level Approach to Reduce the Impact of NBTI on Processor Functional Units", GLSVLSI, May 2010. (Acceptance Rate: 18%)
6. T. Siddiqua, S. Gurumurthi, "Balancing Soft Error Coverage with Lifetime Reliability in Redundantly Multithreaded Processors", International Symposium on MASCOTS, September 2009. (Acceptance Rate: 20%)
7. T. Siddiqua, S. Gurumurthi, "NBTI-Aware Dynamic Instruction Scheduling", IEEE Workshop on Silicon Errors in Logic - System Effects, March 2009.

▪ Other Publications:

1. T. Siddiqua, S. Gurumurthi, "Dynamic NBTI Management in Multicore Processor", ACM Student Research Competition, Grace Hopper Celebration, September 2009.

PROJECTS

- Incorporating BTI in SoC Flow
- Analyzing Flash Reliability
- NBTI-Aware SRAM Structure Design
- Analyzing Circuit-aware Microarchitectural Reliability
- Mutation Resistant Runtime Code using Kernel Attestation
- SimHAT: Simulated Hardware-based Attestation evaluation Tool
- Remote Configuration, Management&Usage of Sensor Network using GSM-enabled Devices
- Implementation of different layers of OSI model using serial port
- Voice recognition software
- Design/implementation of an 8-bit μ processor, ALU, Multiplier & network interface card

COMPUTER SKILLS

- **Languages:** C, C++, Java, Prolog, 80x86 Assembly language
- **Database:** MySQL, MS-SQL Server, MS Access, Oracle
- **Operating Systems:** Windows, LINUX, DOS
- **Graphics Library:** OpenGL
- **Web Development Language:** HTML, ASP, XML, PHP
- **Programming Environments:** MSVisual Studio.NET, Turbo C++, Kawa, Eclipse Platform
- **Simulators:** M5, SimpleScalar, Wattch, HotSpot, Cadence tools

GRADUATE COURSES TAKEN

- Computer Architecture, Theory of Computation, Cyber-Physical Systems, Algorithms, Statistics for Engineers and Scientists, VLSI design, Operating Systems, Advanced VLSI Systems Design, Non-Volatile Memory Systems, Dependable Computing Systems, ASIC/SOC Design

SERVICE

- Reviewer, DAC'2012, ISCAS'2012, TC'2011, TVLSI'2011, ISVLSI'2011, DAC'2010, CAL'2010, ICCAD'2009