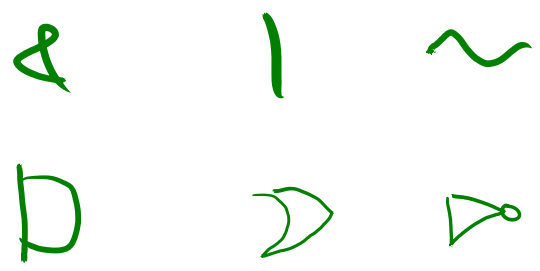


# Transistors

gates



MUX

multi-bit values  
int

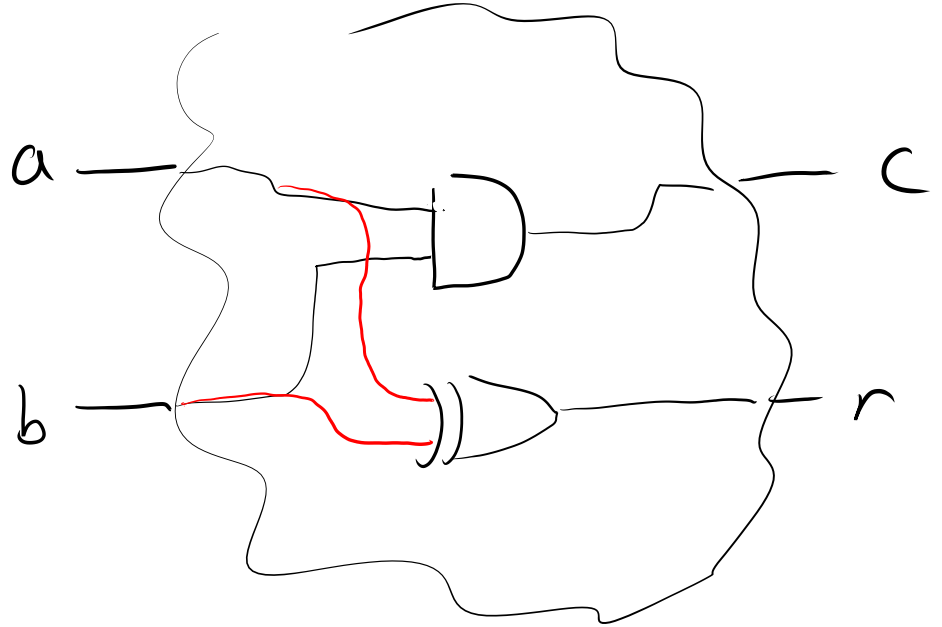
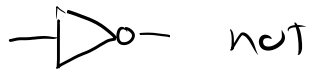
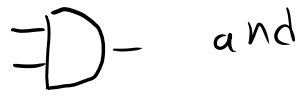
2's comp

IEEE-style

float

# adder

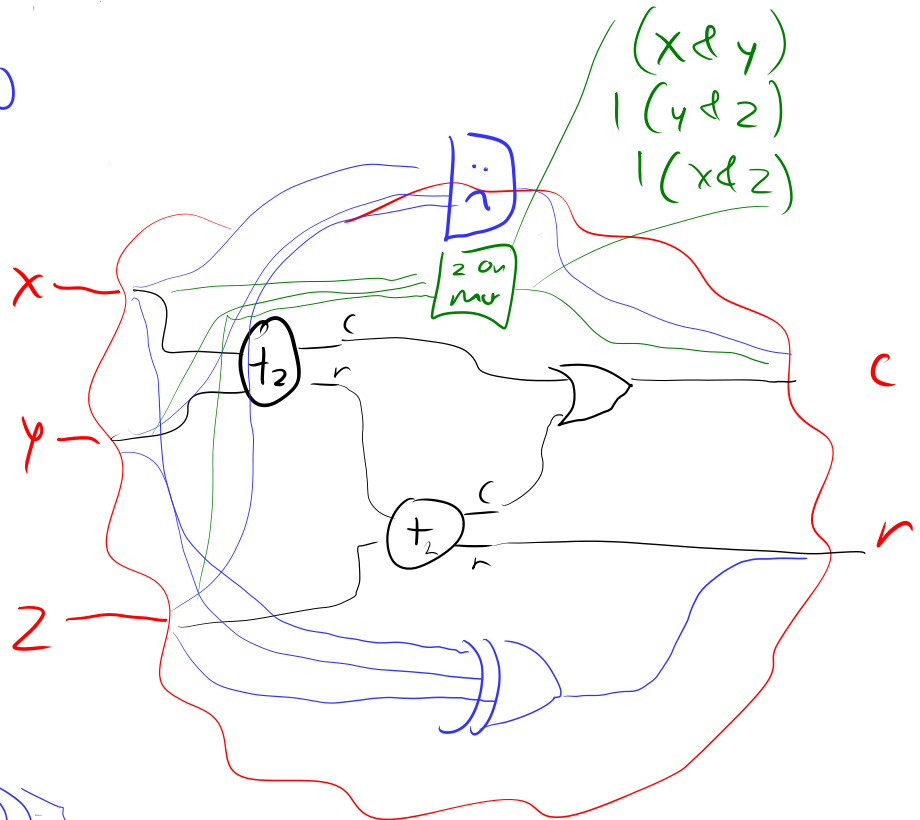
$$\begin{array}{r} a \\ + b \\ \hline cr \end{array}$$

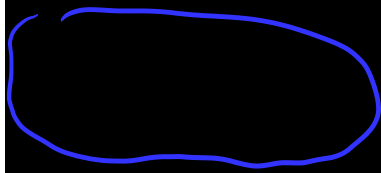
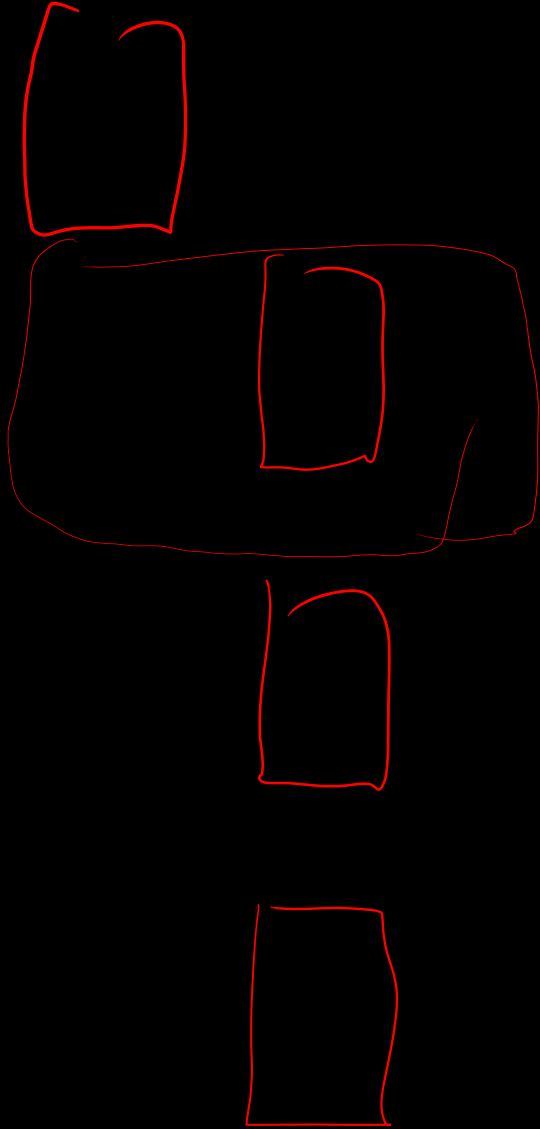


0

odd  $\rightarrow 1$   
Parity even  $\rightarrow 0$

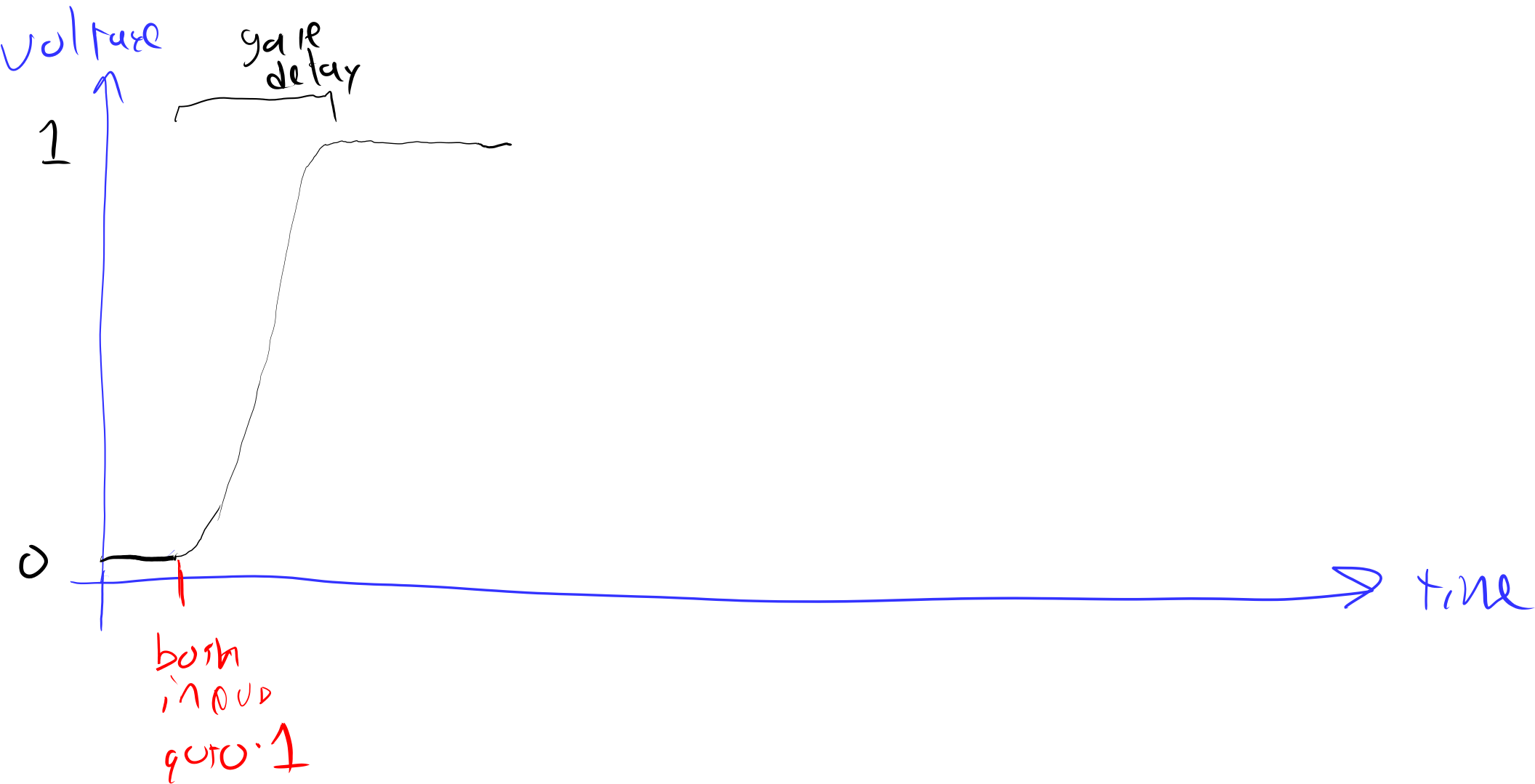
$$\begin{array}{r} x \\ y \\ z \\ \hline cr \end{array}$$



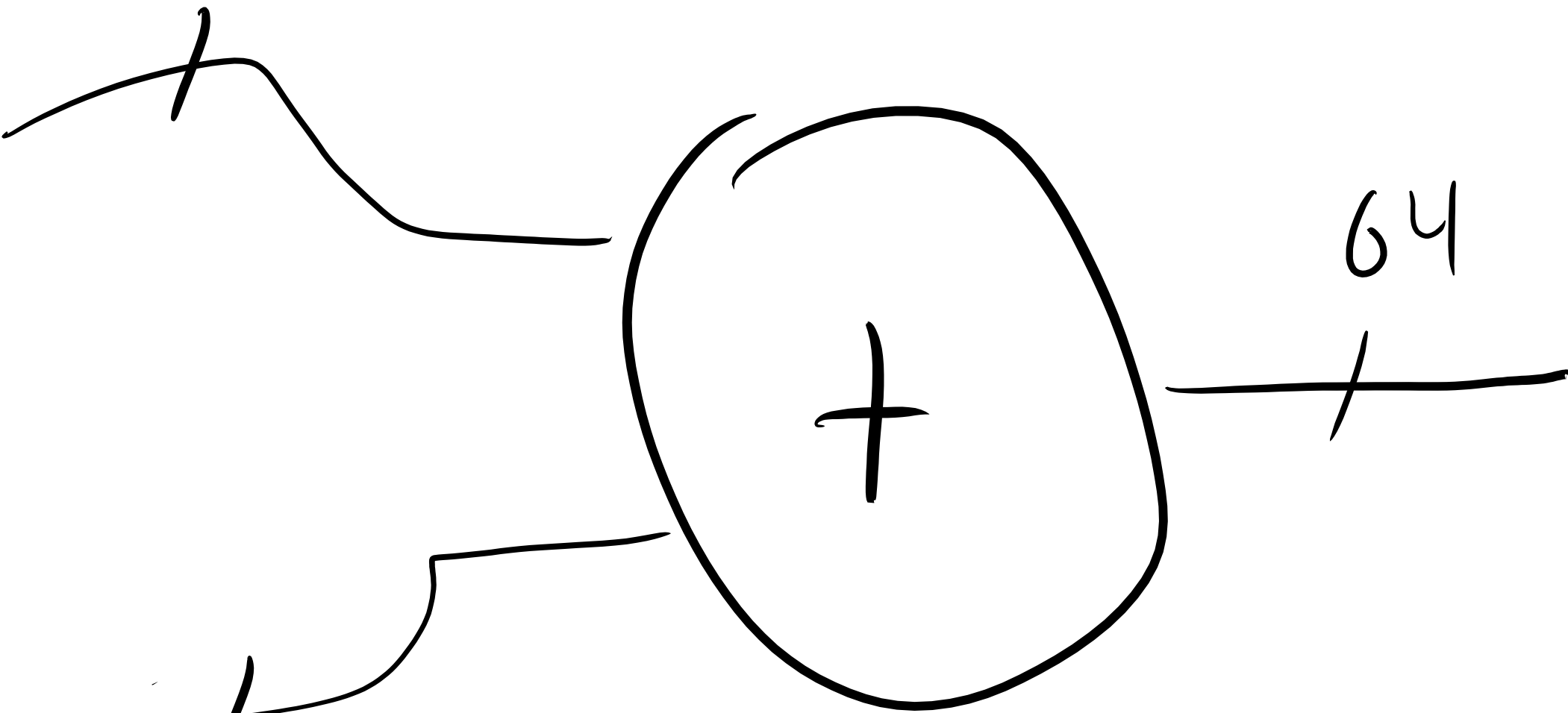


3-bit XOR

and gap



64



64

64

# Computer

✓ mark

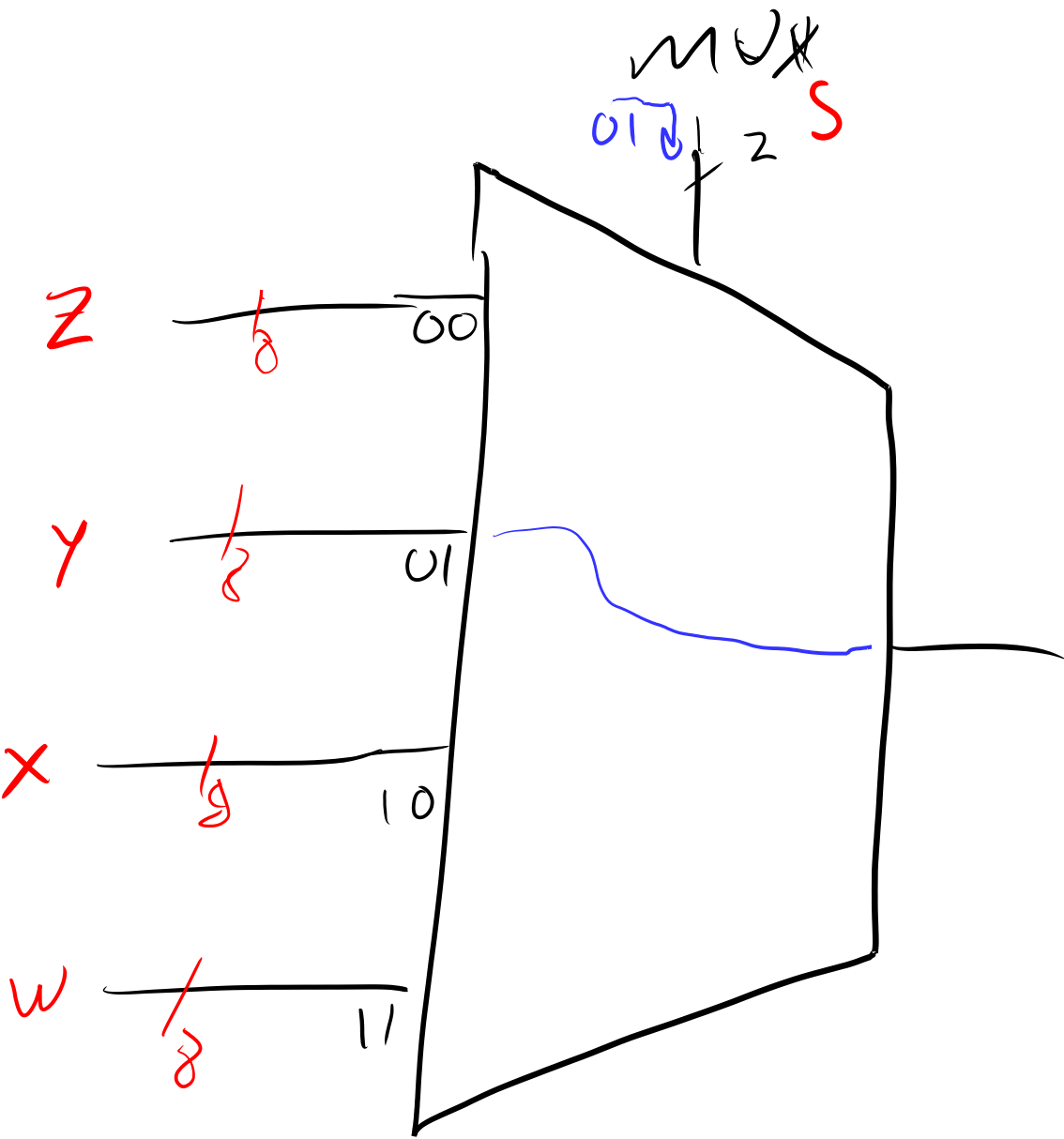
memory

repeated change

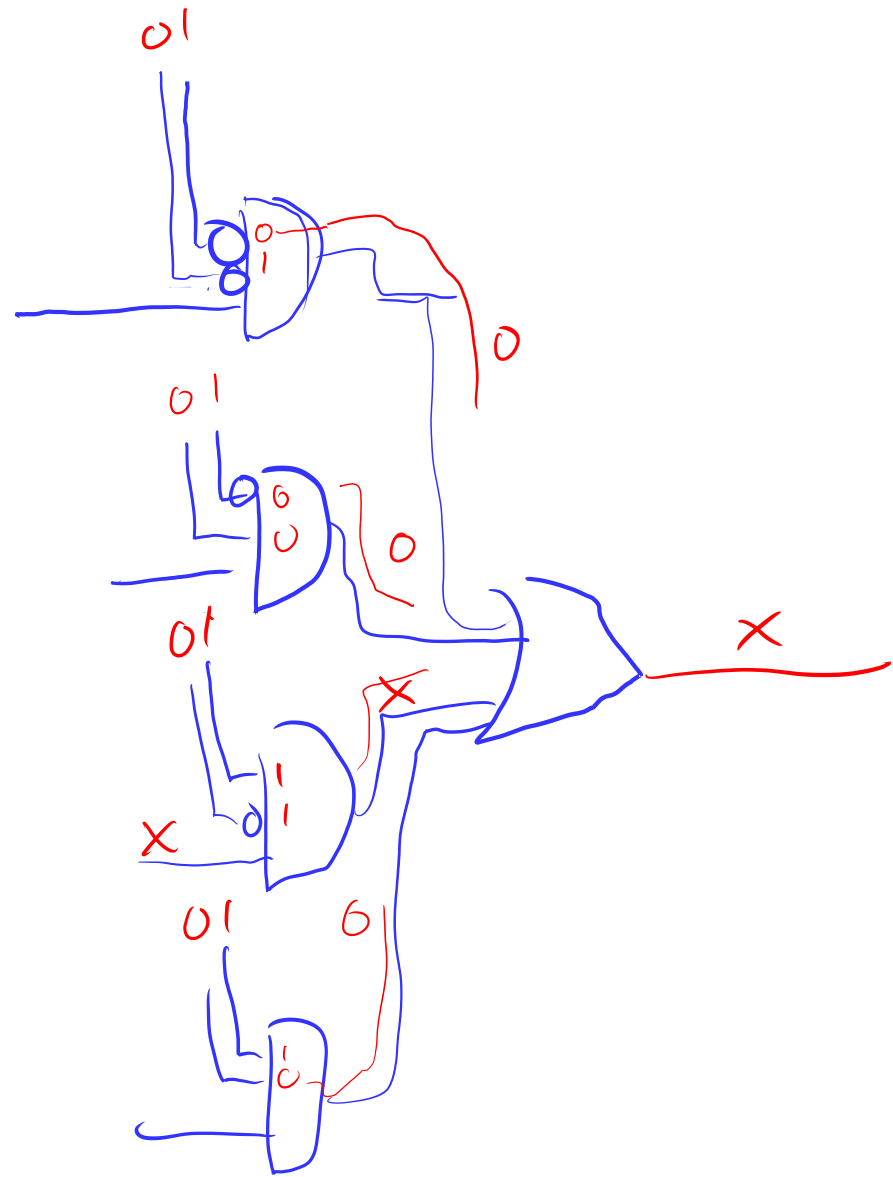
Conditionals

— and then

— mux

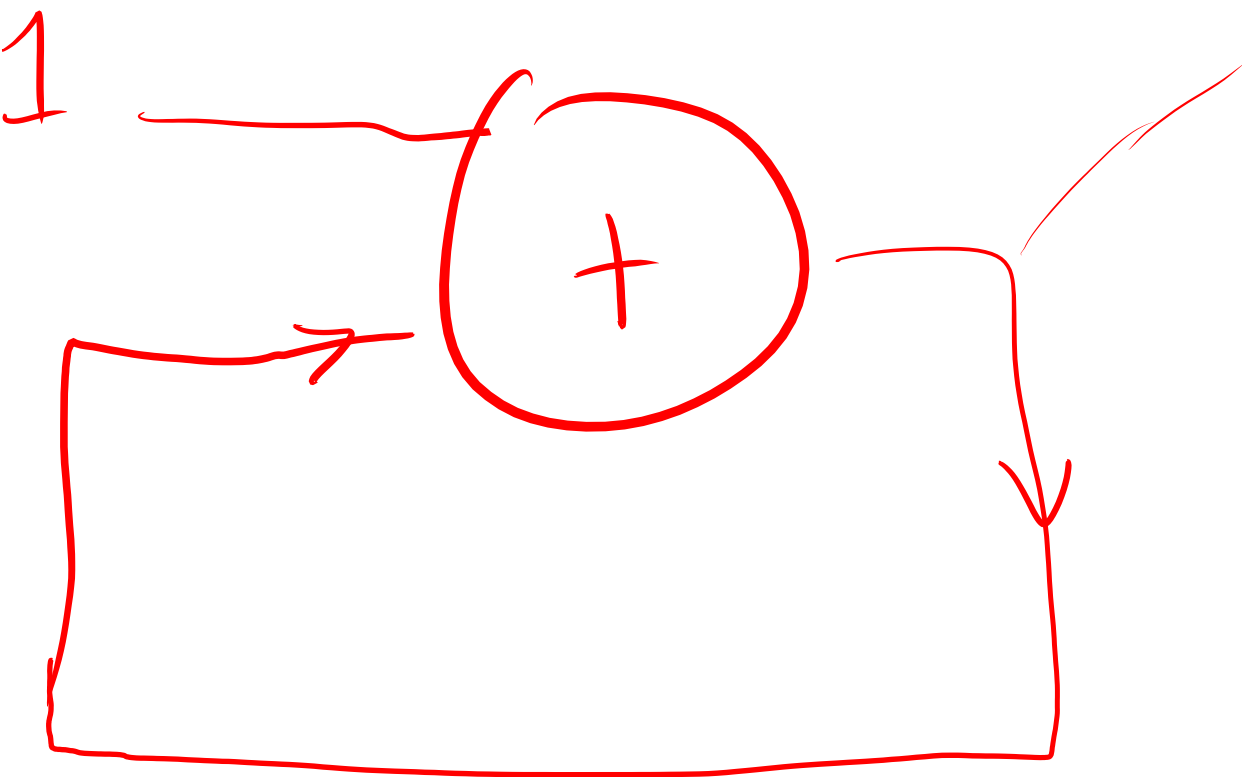


$[z, y, x, w] [s]$



$\vdots \times 8$





init

0

1

2

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011

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010

Problem...