Ashish Venkat

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Professional Appointments

University of Virginia **Aug 2018-Present**
Assistant Professor, Department of Computer Science

University of California, San Diego **Apr 2011-Aug 2018**
Research Assistant, Department of Computer Science

IBM Research Labs, Haifa, Israel **Aug 2016-Dec 2016**
Research Intern, Cloud Platforms Division

Microsoft Research, Redmond, WA **Mar 2015-Jun 2015**
Research Intern, MSR Technologies Lab

Intel Corporation, Santa Clara, CA **Jun 2012-Sep 2012**
Graduate Technical Intern, Processor Binary Translation Group

Amazon.com, Inc., Seattle, WA **Jun 2011-Sep 2011**
Software Development Intern, Retail Systems Group

Brocade Communications, Bangalore, India **May 2009-Aug 2010**
Software Engineer, Storage Encryption Group

Freescale Semiconductor, Bangalore, India **Jul 2008-May 2009**
Software Engineer, Symbian Middleware Group

Education

PhD., Computer Science **Spring 2018**
Thesis: Breaking the ISA Barrier in Modern Computing.
Advisor: Prof. Dean Tullsen
University of California, San Diego

M.S., Computer Science **Spring 2014**
University of California, San Diego

B.Eng., Computer Science **Spring 2008**
National Institute of Engineering, Mysore, India

Honors and Awards Received

IEEE TCAD Hardware and Embedded Security Top Pick 2021 **Dec 2021**
Selected across all top architecture, security, and VLSI design conferences (DAC, DATE, ICCAD, HOST, VLSI Design, CHES, ETS, VTS, ITC, IEEE S&P, Euro S&P, USENIX Security, ASIA CCS, NDSS, ISCA, HASP, MICRO, ASPLOS, HPCA, ACSAC, and ACM CCS) held between the years 2015-2020, for publication in a Special Issue of IEEE TCAD.

IEEE TCAD Hardware and Embedded Security Top Pick 2020 **Nov 2020**
Selected across all top architecture, security, and VLSI design conferences (DAC, DATE, ICCAD, HOST, VLSI Design, CHES, ETS, VTS, ITC, IEEE S&P, Euro S&P, USENIX Security, ASIA CCS, NDSS, ISCA, HASP, MICRO, ASPLOS, HPCA, ACSAC, and ACM CCS) held between the years 2014-2019, for publication in a Special Issue of IEEE TCAD.

IEEE Micro Top Pick 2019 **May 2019**
Selected across all top architecture conferences (ISCA, ASPLOS, MICRO, HPCA) held in 2018, for publication in a Special Issue of IEEE Micro.

HPCA Best Paper Award Runner-Up 2019 **Feb 2019**
Best Paper Runner-Up at a top Computer Architecture conference with an acceptance rate of 21%.

ACM SIGARCH Student Scholarship **June 2012**
One of the seven SIGARCH student scholars to attend the *ACM Turing Centenary Celebrations.*

TEQIP Best Undergraduate Student Project **June 2008**
Awarded by the TEQIP foundation, Government of India.

Significant Press and Coverage

Research on micro-op cache vulnerability published at ISCA 2021 was covered widely by multiple international technology news and mainstream media outlets in **May 2021**.

Research on Composite-ISA Cores published at HPCA 2019 was covered on Coreteks, in the **Aug 2020** article "AMD Master Plan Pt. 2 -- Heterogeneous Revolution".

Research on the Packet Chasing Attack that exploits a new vulnerability in Intel processors was listed by NIST in **Sep 2019** as a medium severity vulnerability under CVE-2019-11184.

Publications

Top Conferences in Computer Architecture: ISCA, ASPLOS, HPCA, MICRO

Speculative Code Compaction: Eliminating Dead Code via Speculative Microcode Transformations
Logan Moody, Wei Qi, Abdolrasoul Sharifi, Layne Berry, Joey Rudek, Jayesh Gaur, Jeff Parkhurst, Sreenivas Subramoney, Kevin Skadron, **Ashish Venkat**,
In *Proceedings of the 55th ACM/IEEE International Symposium on Microarchitecture **(MICRO)***, October, 2022. (19 pages)
Acceptance Rate: 23%

DRAM-CAM: General-Purpose Bit-Serial Exact Pattern Matching
Lingxi Wu, Rasool Sharifi, **Ashish Venkat**, Kevin Skadron,
In *IEEE Computer Architecture Letters **(IEEE CAL)***, Issue 2, Jul-Dec, 2022. (4 pages)
Impact Factor: 2.118

ProxyVM: A Scalable and Retargetable Compiler Framework for Privacy-Aware Proxy Workload Generation
Xida Ren, Alif Ahmed, Yizhou Wei, Kevin Skadron, **Ashish Venkat**,
In *Semiconductor Research Corporation's Annual Technical Conference* ***(SRC TECHCON)***, September, 2022. (5 pages)

SecSMT: Securing SMT Processors against Contention-Based Covert Channels
Mohammadkazem Taram, Xida Ren, **Ashish Venkat**, Dean M. Tullsen,
In *Proceedings of the 31st USENIX Security Symposium* ***(USENIX Security)***, Aug, 2022. (19 pages)
Acceptance Rate: 17%

I See Dead µops: Leaking Secrets via Intel/AMD µop Caches
Xida Ren, Logan Moody, Mohammadkazem Taram, Matthew Jordan, Dean M. Tullsen, **Ashish Venkat**.
In *Proceedings of the 48th International Symposium on Computer Architecture* ***(ISCA)***, June 2021. (14 pages)
Acceptance Rate: 18%

Sieve: A Scalable In-Situ DRAM-based Accelerator for Massively Parallel K-mer Matching
Lingxi Wu, Rasool Sharifi, Marzieh Lenjani, Kevin Skadron, and **Ashish Venkat**.
In *Proceedings of the 48th International Symposium on Computer Architecture* ***(ISCA)***, June 2021. (14 pages)
Acceptance Rate: 18%

CHEx86: Context-Sensitive Enforcement of Memory Safety via Microcode-Enabled Capabilities.
Rasool Sharifi and **Ashish Venkat**.
In *Proceedings of the 47th International Symposium on Computer Architecture* ***(ISCA)***, pages 762-775, June 2020. (14 pages)
Acceptance Rate: 18%
Selected for IEEE TCAD Hardware and Embedded Security Top Picks, 2021!

ProxyVM: A Scalable and Re-Targetable Compiler Framework for Privacy-Preserving Machine Learning
Xida Ren, Jianhui Sun, Kevin Skadron, Aidong Zhang, **Ashish Venkat**.
In the 4th IBM IEEE CAS/EDS AI Compute Symposium, October 2021.

Agon: A Scalable Competitive Scheduler for Large Heterogeneous Systems.
Andreas Prodromou, **Ashish Venkat**, Dean M. Tullsen.
arXiV preprint, 2021

Packet Chasing: Observing Network Packets over a Cache Side-Channel.
Mohammadkazem Taram, **Ashish Venkat**, and Dean M. Tullsen.
In *Proceedings of the 47th International Symposium on Computer Architecture* ***(ISCA)***, pages 721-734, June 2020. (14 pages)
Acceptance Rate: 18%

Platform-Agnostic Learning-Based Scheduling
Andreas Prodromou, **Ashish Venkat**, and Dean M. Tullsen.
In *Proceedings of the 19th International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS)*, pages 142-154, July, 2019. (13 pages). **Acceptance Rate: 38%**

Context-Sensitive Decoding: On-Demand Microcode Customization for Security and Energy Management
Mohammadkazem Taram, **Ashish Venkat**, Dean M. Tullsen.
In ***IEEE Micro***, *Special Issue on the Top Picks from the Computer Architecture Conferences*, pages 75-83, May 2019.
(9 pages). **Impact Factor: 2.57**
Special Issue Acceptance Rate: 9%,
Theme Article!

Context-Sensitive Fencing: Securing Speculative Execution via Microcode Customization.
Mohammadkazem Taram, **Ashish Venkat**, and Dean M. Tullsen.
In *Proceedings of the 24th International Conference on Architectural Support for Programming Languages and Operating Systems **(ASPLOS)***, pages 395-410, April 2019. (16 pages). **Acceptance Rate: 21%.**
Selected for IEEE TCAD Hardware and Embedded Security Top Picks, 2020!

Fast and Efficient Deployment of Security Defenses Via Context Sensitive Decoding
Mohammadkazem Taram, Dean M. Tullsen, **Ashish Venkat**, Houman Homayoun, and Sai Manoj PD.
In *Proceedings of the 44th Government Microcircuit Applications and Critical Technology Conference (GOMACTech)*, March 2019. (6 pages). Government Conference – Acceptance Rate not available.

Composite-ISA Cores: Enabling Multi-ISA Heterogeneity using a Single ISA.
Ashish Venkat, Harsha Basavaraj, and Dean M. Tullsen.
In *Proceedings of the 25th International Symposium High Performance Computer Architecture **(HPCA)***, pages 42-55, February 2019. (14 pages). **Acceptance Rate: 21%. Best Paper Award Runner-Up!**

Deciphering Predictive Schedulers for Heterogeneous-ISA Architectures
Andreas Prodromou, **Ashish Venkat**, Dean M. Tullsen.
In *Proceedings of the 10th International Workshop on Programming Models and Applications for Multicores and Manycores (PMAM)*, February, 2019. (10 pages).
Acceptance Rate: 53%

Mobilizing the Micro-Ops: Exploiting Context-Sensitive Decoding for Security and Energy Efficiency.
Mohammadkazem Taram, **Ashish Venkat**, and Dean M. Tullsen.
In *Proceedings of the 45th International Symposium on Computer Architecture **(ISCA)***, pages 624-637, June 2018. (14 pages)
Acceptance Rate: 17%. Selected for IEEE Micro Top Picks, 2019!

Reliability-Aware Data Placement for Heterogeneous Memory Architecture.
Manish Gupta, Vilas Sridharan, David Roberts, Andreas Prodromou, **Ashish Venkat**, Dean M. Tullsen, and Rajesh Gupta.
In *Proceedings of the 24th International Symposium on High Performance Computer Architecture **(HPCA)***, pages 583-595, February 2018. (13 pages). **Acceptance Rate: 21%**

HIPStR: Heterogeneous-ISA Program State Relocation.
Ashish Venkat, Sriskanda Shamasunder, Hovav Shacham, and Dean M. Tullsen.
In *Proceedings of the 21st International Conference on Architectural Support for Programming Languages and Operating Systems **(ASPLOS)***, pages 727-741, April 2016. (15 pages). **Acceptance Rate: 22%**

Harnessing ISA Diversity: Design of a Heterogeneous-ISA Chip Multiprocessor.
Ashish Venkat and Dean M. Tullsen.
In *Proceedings of the 41st International Symposium on Computer Architecture **(ISCA)***, pages 121-132, June 2014. (12 pages)
Acceptance Rate: 18%

Execution Migration in a Heterogeneous-ISA Chip Multiprocessor.
Matthew DeVuyst, **Ashish Venkat**, and Dean M. Tullsen.
In *Proceesings of the 17th International Conference on Architectural Support for Programming Languages and Operating Systems **(ASPLOS)***, pages 261-272, March, 2012. (12 pages). **Acceptance Rate: 21%**

Patents

Binary Translation-Driven Program State Relocation.
Ashish Venkat, Arvind Krishnaswamy, Yamada Koichi, and Rajan Palanivel.
In *United States Patent Grant US009135435 B2*, September, 2015.

Graduate Students Research Advising

Lingxi Wu (Spring 2020-Present, co-advised by Kevin Skadron)
Milestones: Qualifying Exam Defense Completed.

Xida Ren (Fall 2019-Present)
Milestones: Qualifying Exam Defense Completed.

Logan Moody (Fall 2020-Present)
Milestones: Qualifying Exam Proposal Completed.

ArnabJyoti Kalita (Fall 2022-Present)

Alenkruth Krishnan Murali (Fall 2022-Present)

Saket Upadhyay (Fall 2022-Present)

Yilong Yang (Fall 2022-Present)

Conner Ward (Spring 2022-Present)

Uday Kiran (Fall 2022-Present)

Undergraduate Students Research Advising

Edward Lue (Fall 2022-Present)

Karan Singh (Fall 2022-Present)

Dhruv Pandya (Fall 2022-Present)

Research Advisees Graduated

Virginia Layne Berry (Summer 2019-Fall 2020)
Placement: Ph.D. at University of Texas, Austin
Significant Achievements: **CRA Outstanding Undergraduate Researcher Award Honorable Mention**

Joey Rudek (Summer 2020-Spring 2021)
Placement: Ph.D. at University of California, San Diego

Muhammad Abdullah (Fall 2021-Spring 2022)
Placement: Capital One

Grants

NSF PPoSS *Oct 2022 – Sep 2027*
Co-designing Hardware, Software, and Algorithms to Enable Extreme-Scale Machine Learning Systems
Role: Co-Principal Investigator.
Funding Amount (total): $3,000,000

NSF CCRI *Oct 2022 – Sep 2025*
A Scalable Hardware and Software Environment Enabling Secure Multi-party Learning
Role: Co-Principal Investigator.
Funding Amount (total): $1,120,000

SRC CADT *Jan 2022 – Dec 2024*
A Scalable and Re-Targetable Compiler Framework for Privacy-Preserving Machine Learning
Role: Principal Investigator.
Funding Amount: $297,000

NSF CCF: SHF *Feb 2020 – Jan 2021*
Student Travel Grant for the 26th IEEE International Symposium on High Performance Computer Architecture (HPCA 2020)
Role: Principal Investigator
Funding Amount: $20,000

NSF/Intel Foundational Microarchitecture Research (FoMR) *Oct 2019 – Sep 2023*
Speculative Super-optimization: Boosting Performance via Speculation-Driven Dynamic Binary Optimization
Role: Principal Investigator.
Funding Amount (total): $416,000

NSF CRII: SaTC *Mar 2019 – Feb 2022*
Mitigating Software-Based Microarchitectural Attacks via Secure Microcode Customization
Role: Principal Investigator
Funding Amount: $174,996

DARPA MTO: SSITH *Dec 2018 – Mar 2021*
Mobilizing the Micro-Ops: Securing Processor Architectures via Context-Sensitive Decoding
Role: Principal Investigator (Sub).
Funding Amount: $1,101,217

Invited Talks

Speculative Code Compaction: Eliminating Dead Code via Speculative Microcode Transformations *Sep 2022*
Intel Labs Worldwide (Virtual Tech Talk)

Mechanism Design for Improving Hardware Security *Aug 2022*
Invited Participant at the CCC Visioning Workshop

Speculative Super-optimization: Boosting Performance via Speculation-Driven Dynamic Binary Optimization *Oct 2021*
Intel Labs Worldwide (Virtual Tech Talk)

I See Dead μops: Leaking Secrets via Intel/AMD μop Caches *Apr 2021*
Intel Labs Worldwide (Virtual Tech Talk)

Speculative Super-optimization: Boosting Performance via Speculation-Driven Dynamic Binary Optimization *Jun 2020*
Intel Labs Worldwide (Virtual Tech Talk)

Fast and Efficient Deployment of Security Defenses via Microcode Customization. *Nov 2019*
University of Cambridge, UK.

Breaking the ISA Barrier in Modern Computing. *Mar 2019*
North Carolina State University, Raleigh.

Composite-ISA Cores: Enabling Multi-ISA Heterogeneity using a Single ISA. *Feb 2019*
HPCA 2019, Best Paper Session.

Mobilizing the Micro-Ops: Exploiting Context-Sensitive Decoding for Performance and Security. *Aug 2018*
Intel Labs, Santa Clara.

Breaking the ISA Barrier in Modern Computing. *May 2018*
Northeastern University, Boston.

Exploiting Multi-ISA Architectures for Security and Efficiency. *April 2017*
Qualcomm, San Diego.

Breaking the ISA Barrier in Modern Computing. *Nov 2016*
Intel Research Lab, Haifa, Israel.

Breaking the ISA Barrier in Modern Computing. *Nov 2016*
Technion, Israel.

HIPStR: Smashing ROP Gadgets via Cross-ISA Process Migration. *Oct 2016*
IBM Haifa Research Lab, Israel.

Breaking the ISA Barrier in Modern Computing. *Aug 2016*
IBM Haifa Research Lab, Israel.

HIPStR: Heterogeneous-ISA Program State Relocation. *Apr 2016*
ASPLOS 2016, Atlanta.

Heterogeneous-ISA Chip Multiprocessors. *Oct 2014*
AMD Research, Sunnyvale.

Harnessing ISA Diversity: Design of a Heterogeneous-ISA Chip Multiprocessor. *Jun 2014*
ISCA 2014, Minneapolis.

Execution Migration in a Heterogeneous-ISA Chip Multiprocessor. *Mar 2012*
ASPLOS 2012, London, UK.

Teaching Experience

Assistant Professor, University of Virginia
CS 6354, Graduate Computer Architecture (Fall 2019, Fall 2021, Fall 2022)
CS 3330, Undergraduate Computer Architecture (Spring 2019, Spring 2020, Spring 2021, Spring 2022)
CS 6501/4501, Hardware Security (Fall 2018, Fall 2020, Spring 2023)

Guest Lecturer
CS 6190, Computer Science Perspectives (Fall 2018, Fall 2019, Fall 2020)
CS 6354, Graduate Computer Architecture (Fall 2018)
CSE 141, Introduction to Computer Architecture at UC San Diego (Winter 2015, Winter 2017).

Internal Departmental/School Service

SEAS Computer Engineering Strategic Committee (2022-2023)

Faculty Search Committee, Systems Area Coordinator (2021-2022)

SEAS Computer Engineering Qualification Exam Committee, Chair (2020-2021)

SEAS Computer Engineering Graduate Program Committee, Member (2020-2021)

Faculty Search Committee, Member (2018-2019)

Computing Systems Committee, Member (2019-2021)

Thesis Defense Committees
Vaibhav Verma, Fall 2021
Marzieh Lenjani, Fall 2020
Reza Rahimi, Fall 2020
Chunkun Bo, Fall 2019
Elaheh Sadredini, Spring 2019 (Chair)

Ph.D. Qualifying Examination Committees
Alif Ahmed, Spring 2021
Alan Wang, Summer 2020
Yipei Song, Summer 2020
Jerry Xing, Summer 2020
Aaron Kinfe, Summer 2020
Qi Liu, Summer 2020
Yujia Mu, Summer 2020
Alif Ahmed, Summer 2020
Lingxi Wu, Spring 2020 (Chair)
Marzieh Lenjani, Fall 2019

Professional Service

Organizing Committee
Student Travel Chair, IEEE/ACM International Symposium on Microarchitecture (MICRO), 2020, 2021, 2022
Student Travel Chair, IEEE International Symposium on High Performance Computer Architecture (HPCA), 2020

Program Committee
IEEE Micro Top Picks, 2021
ACM/IEEE International Symposium on Computer Architecture (ISCA), 2019, 2020, 2021, 2022, 2023
IEEE/ACM International Symposium on Microarchitecture (MICRO), 2022
ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2023
IEEE International Parallel & Distributed Processing Symposium (IPDPS), 2021
IEEE International Symposium on High Performance Computer Architecture (HPCA), 2020
IEEE International Conference on Computer Design (ICCD), 2019, 2021, 2022
ACM International Workshop on Hardware and Architectural Support for Security and Privacy, 2020, 2021, 2022
IEEE International Symposium on Secure and Private Execution Environment Design (SEED), 2021, 2022
ACM Student Research Competition (SRC) in conjunction with ASPLOS, 2019
Young Architect Workshop (YArch) in conjunction with HPCA/ASPLOS, 2019, 2020

NSF Panel
Spring 2020, Spring 2022

External Review Committee
IEEE/ACM International Symposium on Microarchitecture (MICRO), 2020, 2021
ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2020
IEEE International Symposium on Quality Electronic Design (ISQED), 2012

Journal Peer Review
ACM Transactions on Architecture and Code Optimization, 2021
IEEE Transactions on Computers, 2020, 2022
IEEE Micro, Jul-Aug 2015, Jul-Aug 2019, Sep-Oct 2019
IEEE Computer Architecture Letters, 2015, 2019, 2021, 2022
IEEE Transactions on Parallel and Distributed Systems (TPDS), 2017, 2018
IEEE Concurrency and Computation, Practice and Experience (CCPE), 2019
Journal of Systems and Software (JSS), 2015

References

Made available upon request.