last time (1)

sometimes OS needs to handle something

- program did something weird (segfault, divide by zero, ...)
- program asked for OS's help (system call)
- program ran for too long (timer interrupt)
- external keyboard/network/disk/etc. needs attention

exception: hardware mechanism to run OS

- OS sets up *exception table* at boot
- exception table points to *exception handlers*
- hardware calls exception handlers

some operations require kernel mode

- prevents programs from doing 'dangerous' things
- hardware switches to kernel mode on exception
- non-OS code always runs in user mode

last time (2)

programs run with illusion of owning CPU + memory

idea called "process"

thread = illusion of own CPU

- created via *time multiplexing*
- OS performs *context switch* to share CPU between programs over time

address space = illusion of own memory

- created via address translation
- OS sets mapping from virtual (program) to physical (real) addresses
- processor implements mapping

virtual memory

- virtual + physical memory divided into fixed-sized pages
- table: virtual page X $\rightarrow$ (valid?, physical page Y, other info)
- processor does look up in table

quiz Q1 (1)

contiguous chunks of A, B, C — normal load/stores good

```
for (int i = 0; i < 8192; i += 1) {
    A[i] += B[i-1] + B[i] + B[i+1];
}
for (int i = 0; i < 8192; i += 1) {
    for (int j = 0; j < 8192; j += 1) {
        A[i*8192+j] = B[i*8192 + j] * C[j];
    }
}
```

quiz Q1 (2)

not contiguous, vector load/store good

```
for (int i = 0; i < 8192; i += 1) {
    B[i] = A[T[i]];
    // vector of A[T[i]] addresses
}

for (int i = 1 /*typo: was 0 in quiz */;
     i < 8192; i *= 3) {
    A[i] *= B[i];
    // vector of A[1], A[3], A[9], ... addresses
}
```

quiz Q2

```
movq $100, %rax
movq $200, %rcx
addq %rcx, %rax
```

OS switches before addq completes

going to go back starting at addq

so saving value of registers (100, 200) in its memory

quiz Q3

exception table contains pointers to exception handling code

quiz Q4/5

process A: hey, OS, i want to read this file

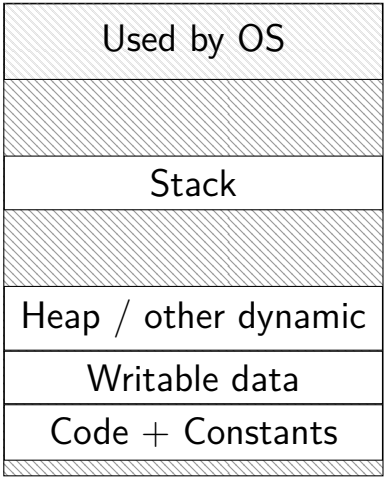
- system call — process A can't talk to disk itself
- OS starts running process B while waiting for data

process B: runs normally

disk finishes, triggers exception to let OS know

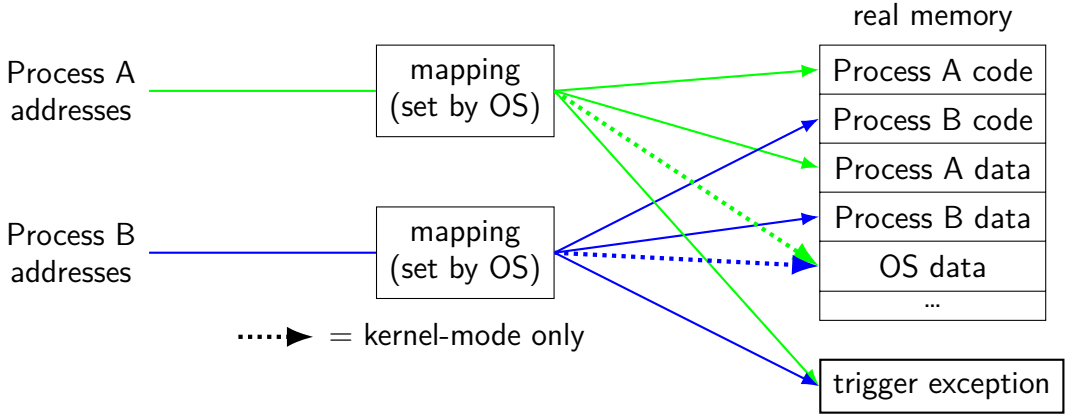
OS switches to process A now

program memory



address spaces

illuision of dedicated memory



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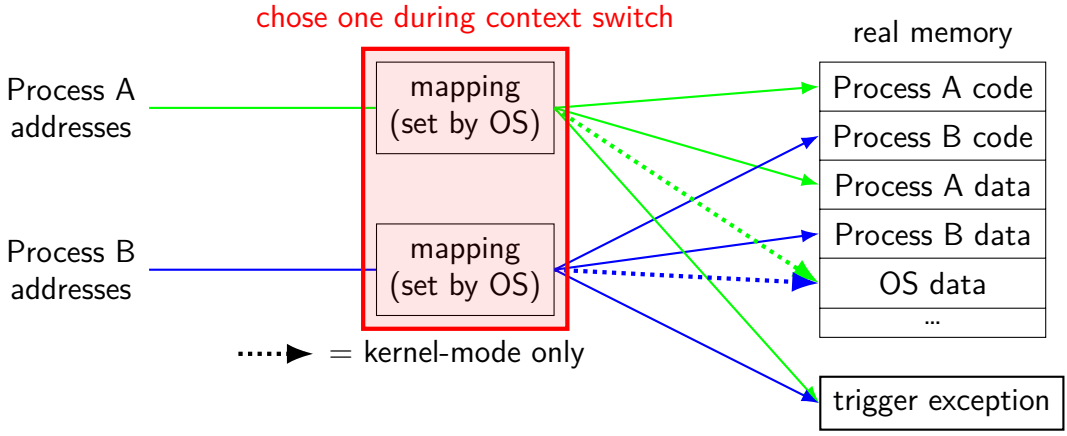
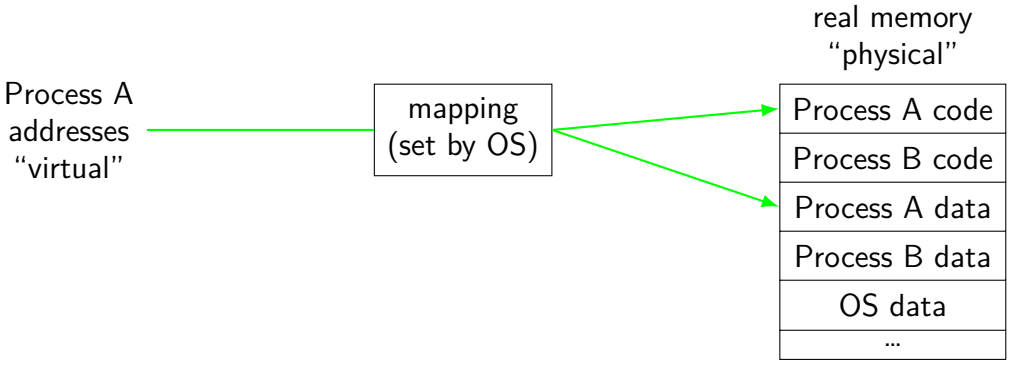
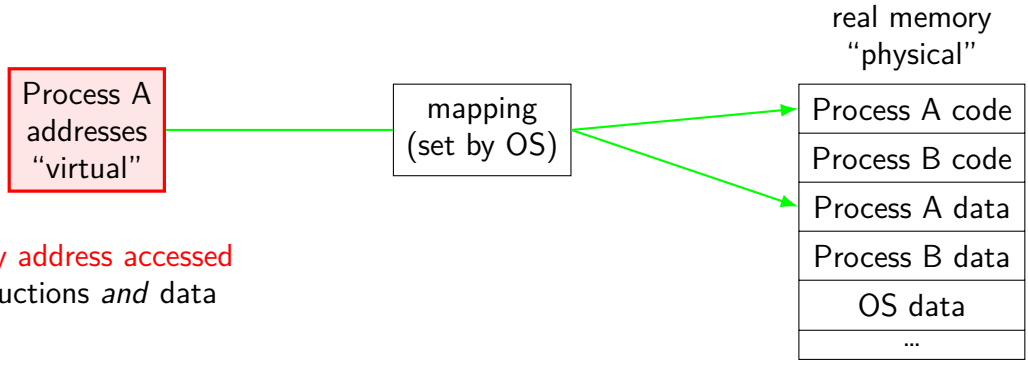


address translation

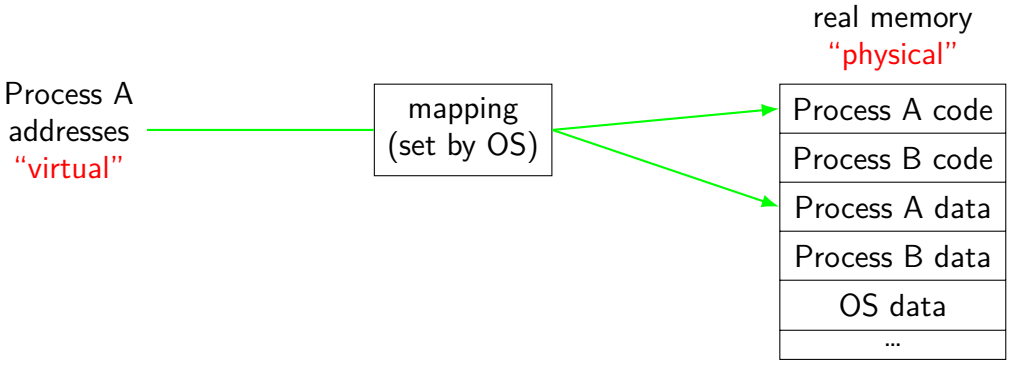


address translation



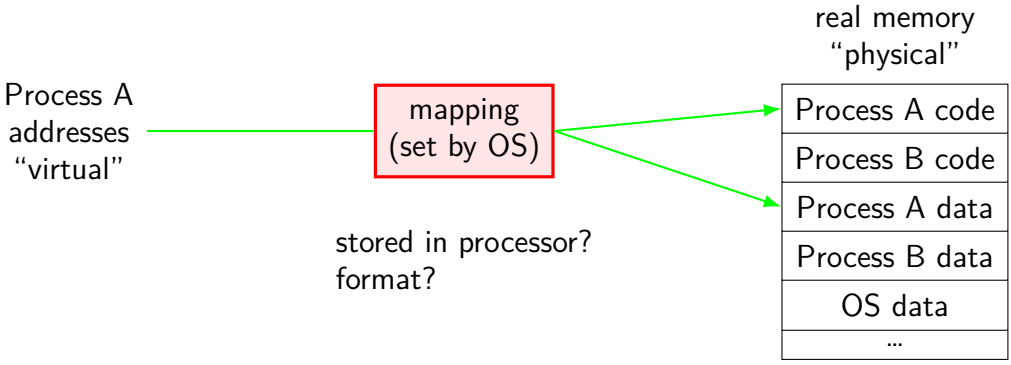
every address accessed
instructions *and* data

address translation

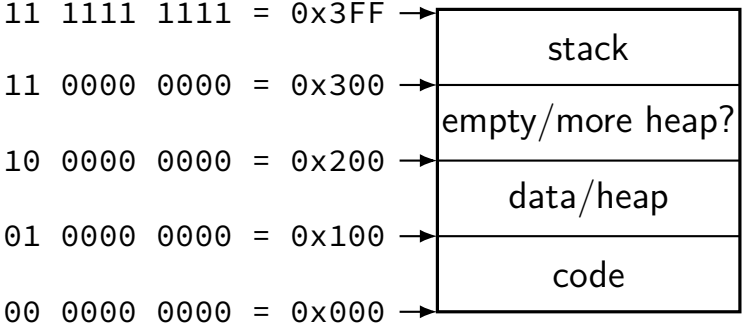


program addresses are 'virtual'
real addresses are 'physical'
can be different sizes!

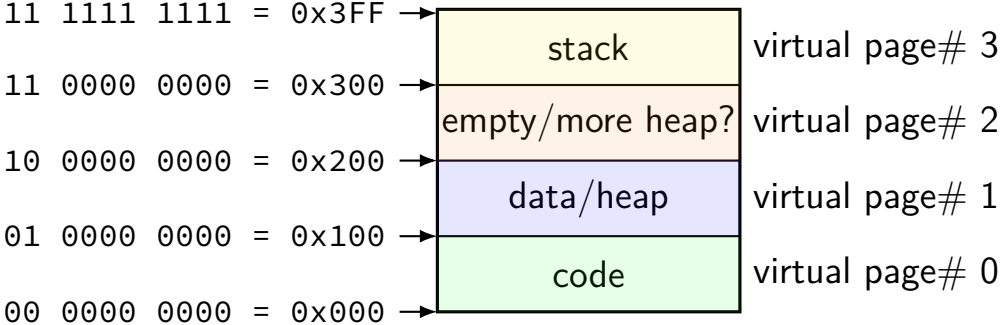
address translation



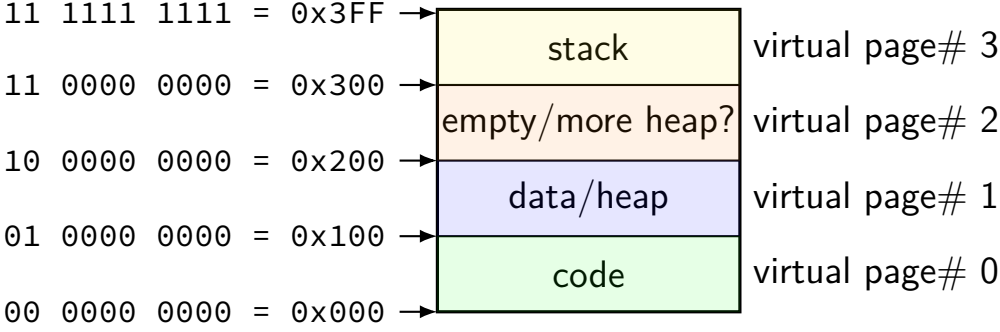
toy program memory



toy program memory

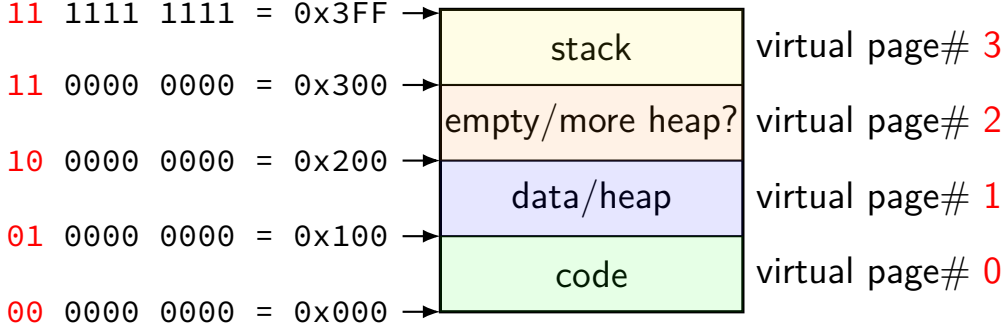


toy program memory



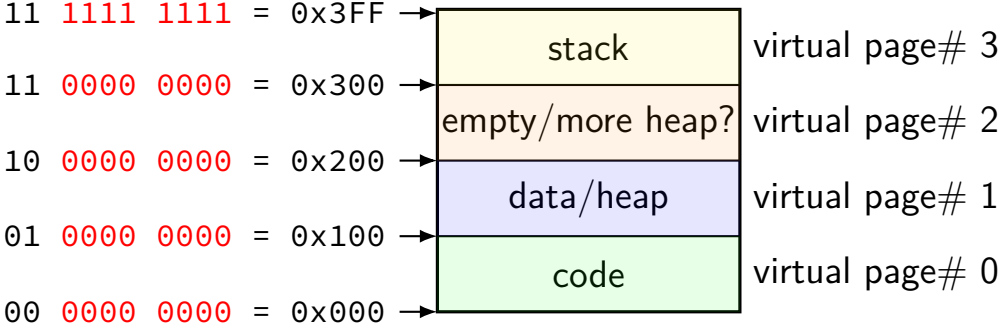
divide memory into pages (2^8 bytes in this case)
"virtual" = addresses the program sees

toy program memory



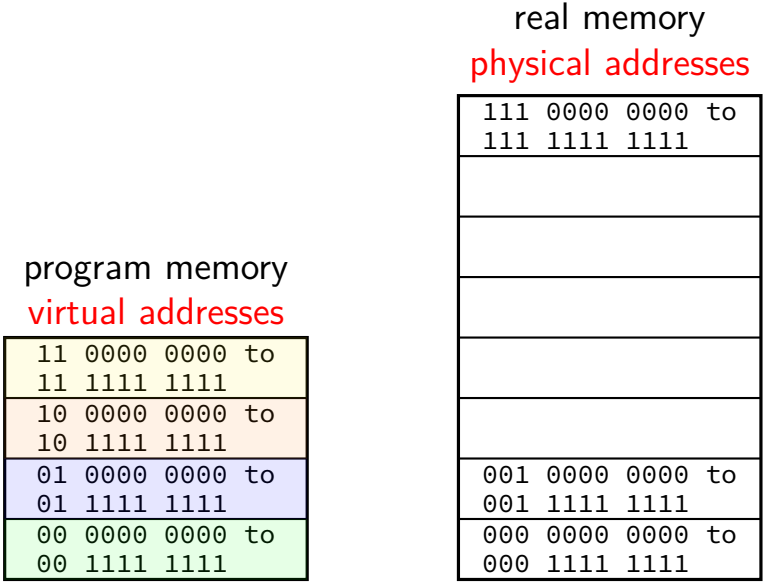
page number is upper bits of address
(because page size is power of two)

toy program memory

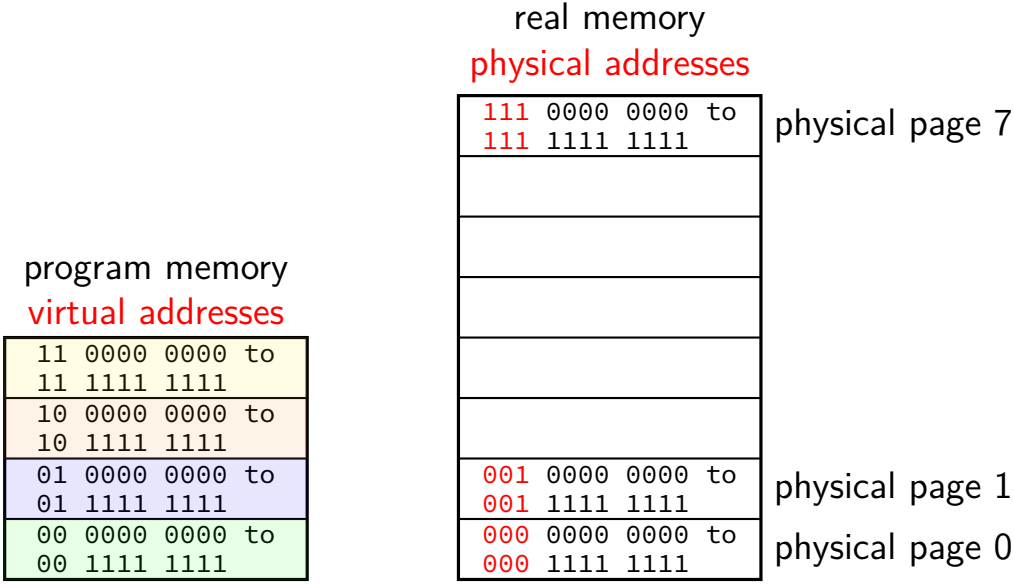


rest of address is called page offset

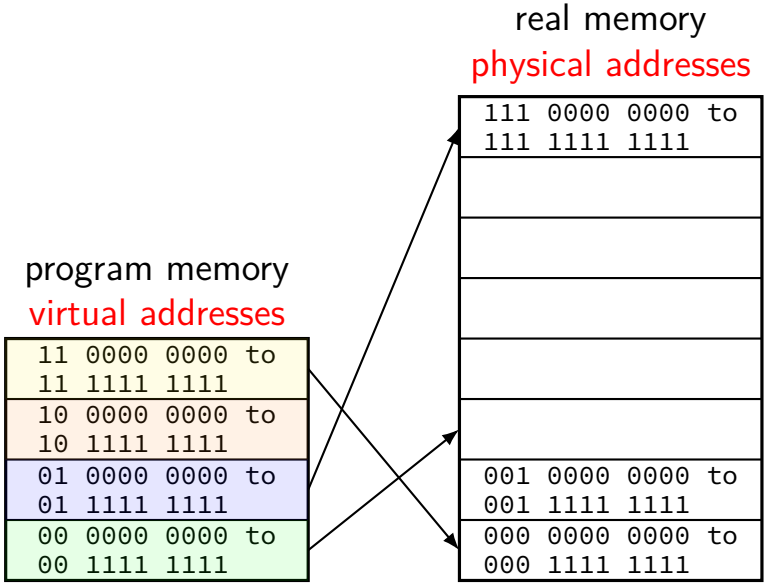
toy physical memory



toy physical memory

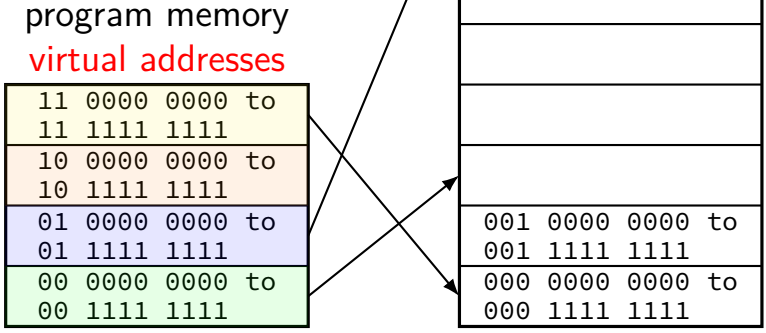


toy physical memory



toy physical memory

virtual page #	physical page #
00	010 (2)
01	111 (7)
10	*none*
11	000 (0)



toy physical memory

page table!

virtual page #	physical page #
00	010 (2)
01	111 (7)
10	*none*
11	000 (0)

program memory

virtual addresses

11 0000 0000 to 11 1111 1111
10 0000 0000 to 10 1111 1111
01 0000 0000 to 01 1111 1111
00 0000 0000 to 00 1111 1111

real memory

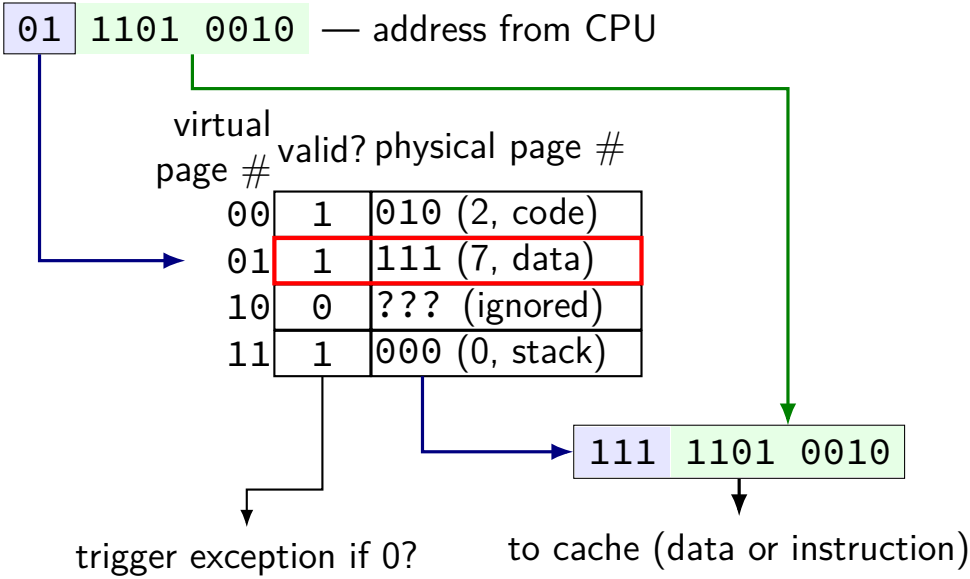
physical addresses

111 0000 0000 to 111 1111 1111
001 0000 0000 to 001 1111 1111
000 0000 0000 to 000 1111 1111

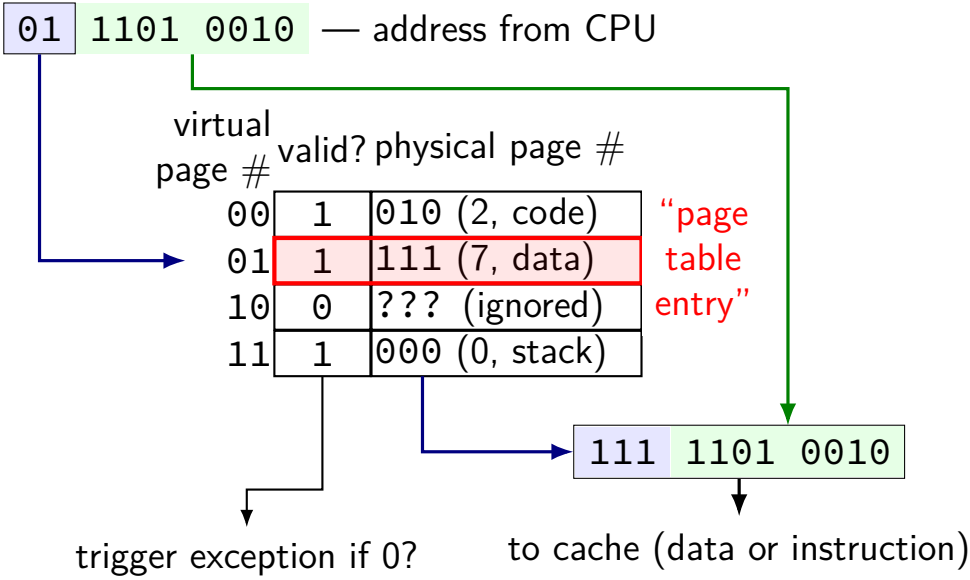
toy page table lookup

virtual page #	valid?	physical page #
00	1	010 (2, code)
01	1	111 (7, data)
10	0	??? (ignored)
11	1	000 (0, stack)

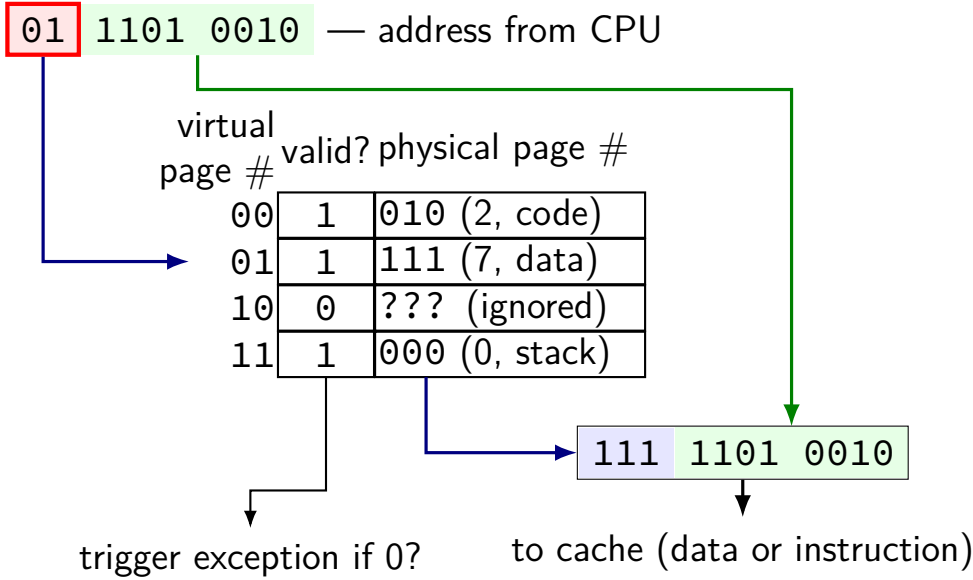
toy page table lookup



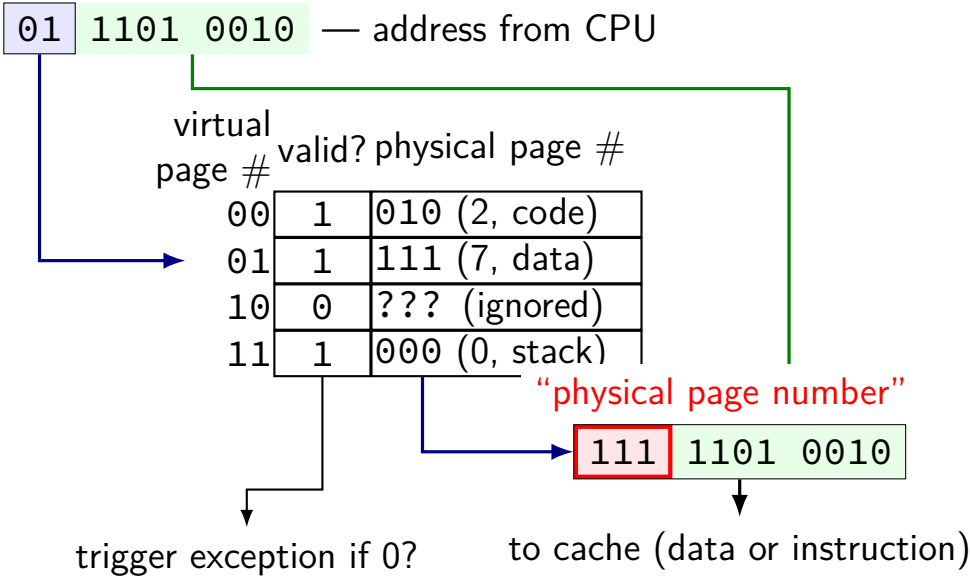
toy page table lookup



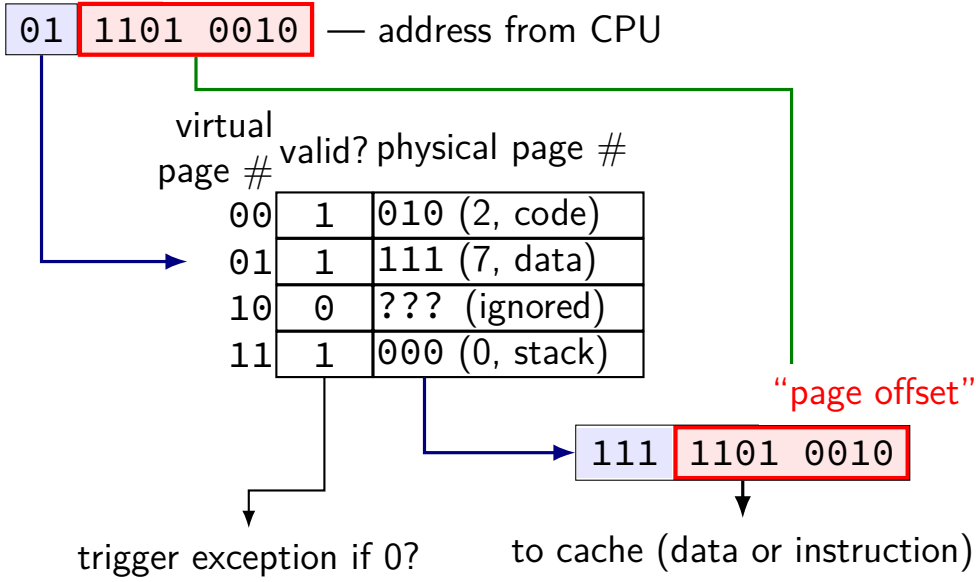
t "virtual page number" lookup



toy page table lookup



toy page lookup



switching page tables

part of context switch is changing the page table

extra privileged instructions

switching page tables

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where in memory is the code that does this switching?

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where in memory is the code that does this switching?

- probably have a page table entry pointing to it
- hopefully marked kernel-mode-only

switching page tables

part of context switch is changing the page table

extra privileged instructions

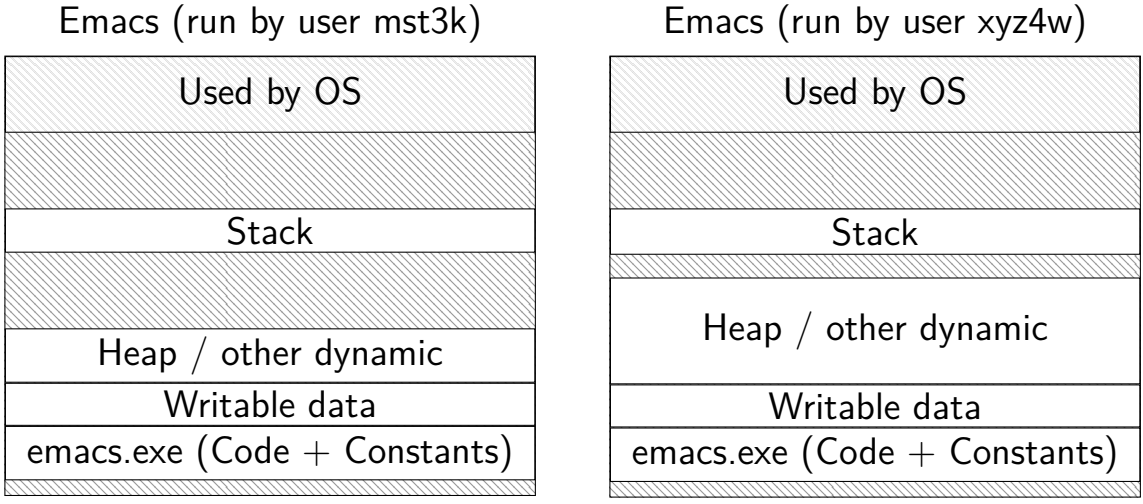
where in memory is the code that does this switching?

- probably have a page table entry pointing to it
- hopefully marked kernel-mode-only

code better not be modified by user program

- otherwise: uncontrolled way to "escape" user mode

emacs (two copies)



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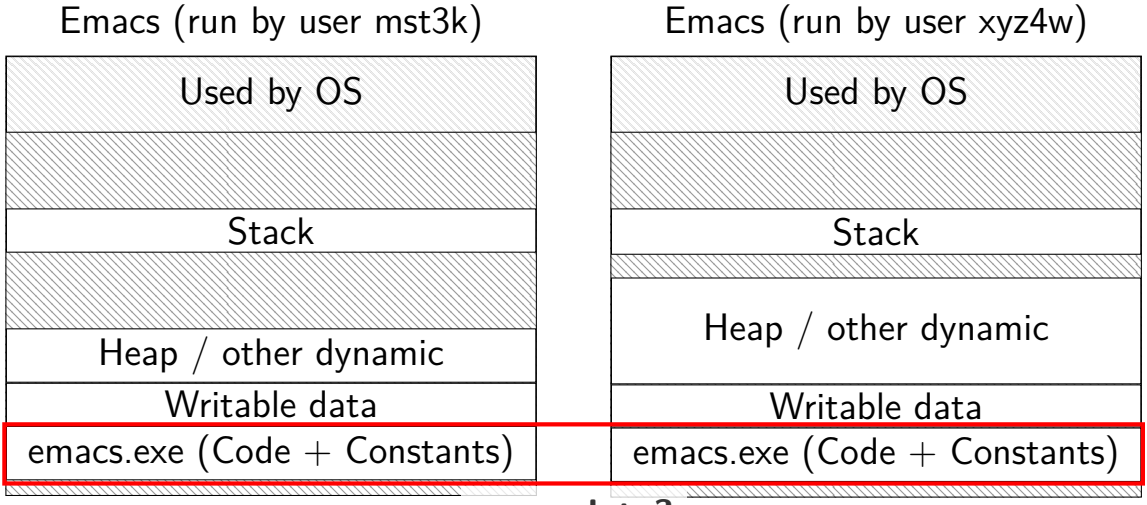


two copies of program

would like to only have one copy of program

what if `mst3k`'s emacs tries to modify its code?

would break process abstraction:

> "illusion of own memory"

typical page table entries

solution: same idea as kernel-only bit

page table entry will have more permissions bits

- can read?
- can write?
- can execute?

checked by MMU like valid/kernel bit

page table (logically)

virtual page #	valid?	kernel?	write?	exec?	physical page #
0000 0000	0	0	0	0	00 0000 0000
0000 0001	1	0	1	0	10 0010 0110
0000 0010	1	0	1	0	00 0000 1100
0000 0011	1	0	0	1	11 0000 0011
...					
1111 1111	1	0	1	0	00 1110 1000

on virtual address sizes

virtual address size = size of pointer?

often, but — sometimes part of pointer not used

example: typical x86-64 only use 48 bits

- rest of bits have fixed value

virtual address size is amount used for mapping

address space sizes

amount of stuff that can be addressed = address space size

- based on number of unique addresses

e.g. 32-bit virtual address = 2^{32} byte virtual address space

e.g. 20-bit physical addresss = 2^{20} byte physical address space

address space sizes

amount of stuff that can be addressed = address space size

- based on number of unique addresses

e.g. 32-bit virtual address = 2^{32} byte virtual address space

e.g. 20-bit physical addresss = 2^{20} byte physical address space

what if my machine has 3GB of memory (not power of two)?

- not all addresses in physical address space are useful
- most common situation (since CPUs support having a lot of memory)

exercise: page counting

suppose 32-bit virtual (program) addresses

and each page is 4096 bytes (2^{12} bytes)

how many virtual pages?

exercise: page counting

suppose 32-bit virtual (program) addresses

and each page is 4096 bytes (2^{12} bytes)

how many virtual pages?

$2^{32}/2^{12} = 2^{20}$

exercise: page table size

suppose 32-bit virtual (program) addresses

suppose 30-bit physical (hardware) addresses

each page is 4096 bytes (2^{12} bytes)

pgae table entries have physical page #, valid bit, kernel-mode bit

how big is the page table (if laid out like ones we've seen)?

exercise: page table size

suppose 32-bit virtual (program) addresses

suppose 30-bit physical (hardware) addresses

each page is 4096 bytes (2^{12} bytes)

pgae table entries have physical page #, valid bit, kernel-mode bit

how big is the page table (if laid out like ones we've seen)?

2^{20} entries $\times(18+2)$ bits per entry

issue: where can we store that?

exercise: address splitting

and each page is 4096 bytes (2^{12} bytes)

split the address `0x12345678` into page number and page offset:

exercise: address splitting

and each page is 4096 bytes (2^{12} bytes)

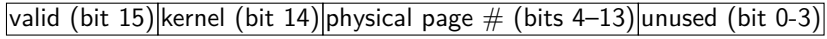
split the address `0x12345678` into page number and page offset:

page #: `0x12345`; offset: `0x678`

page tables in memory

where can processor store megabytes of page tables? in memory

page table entry layout



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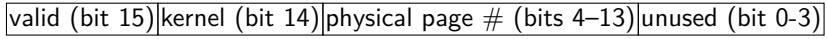


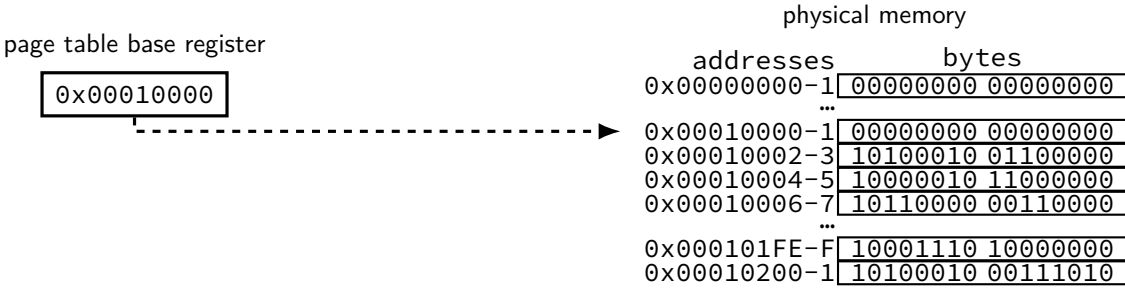
page table base register

page tables in memory

where can processor store megabytes of page tables? in memory

page table entry layout

valid (bit 15)	kernel (bit 14)	physical page # (bits 4–13)	unused (bit 0-3)



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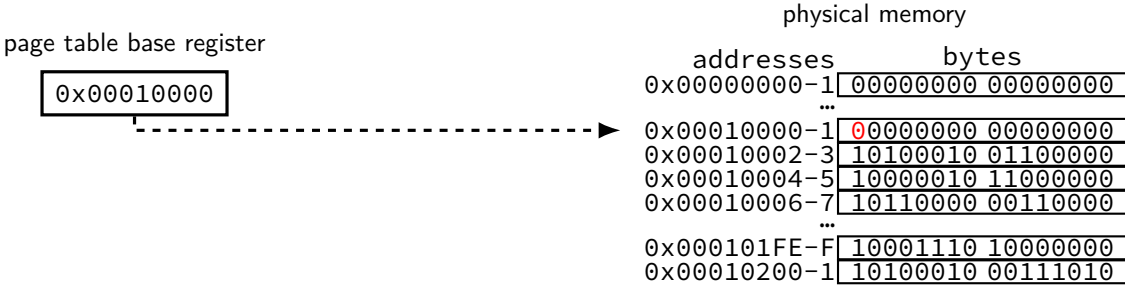

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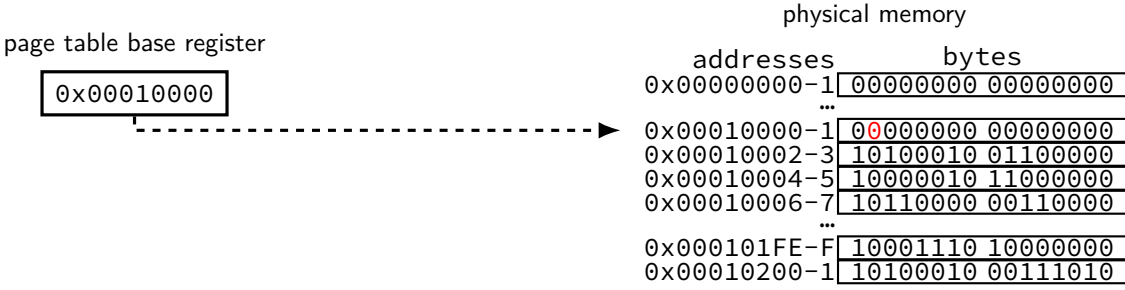

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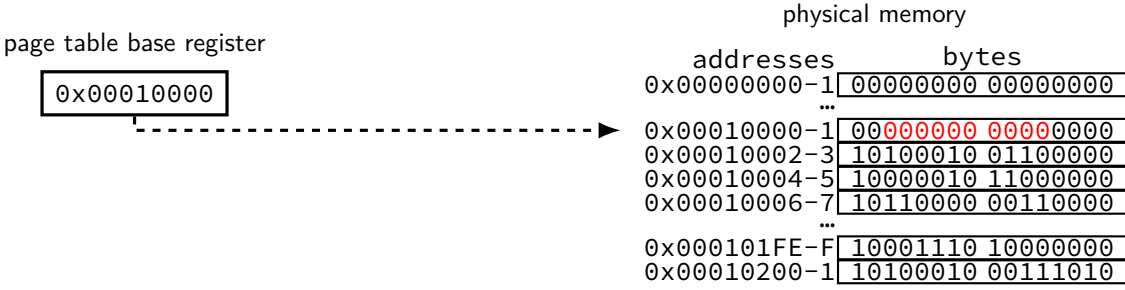

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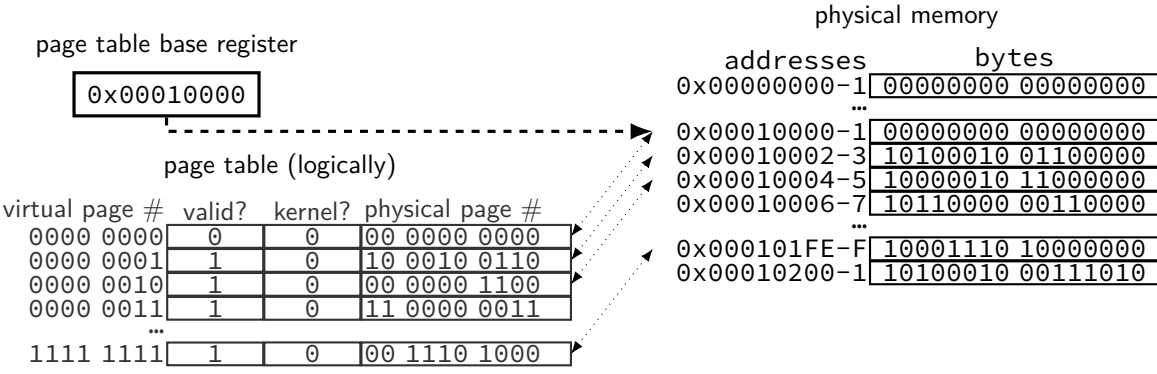

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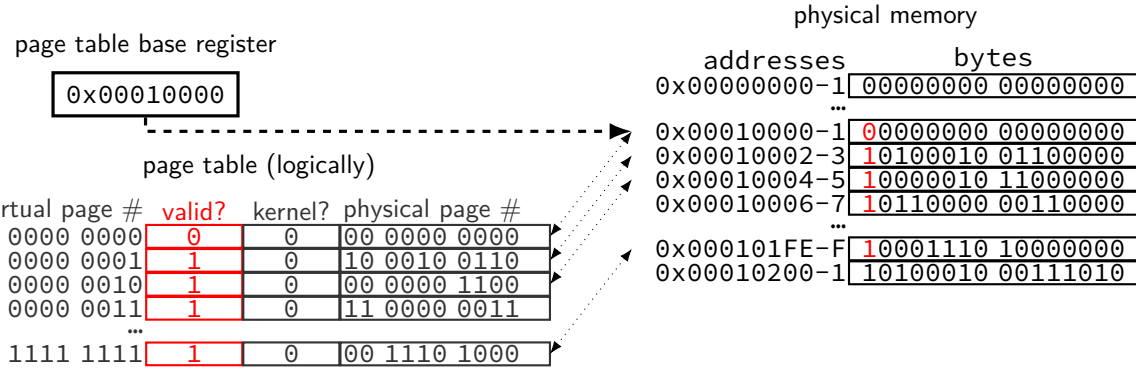

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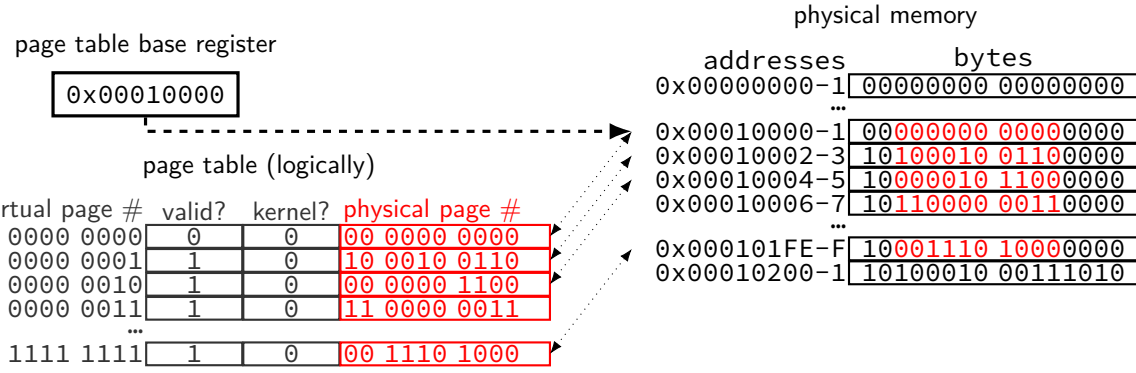

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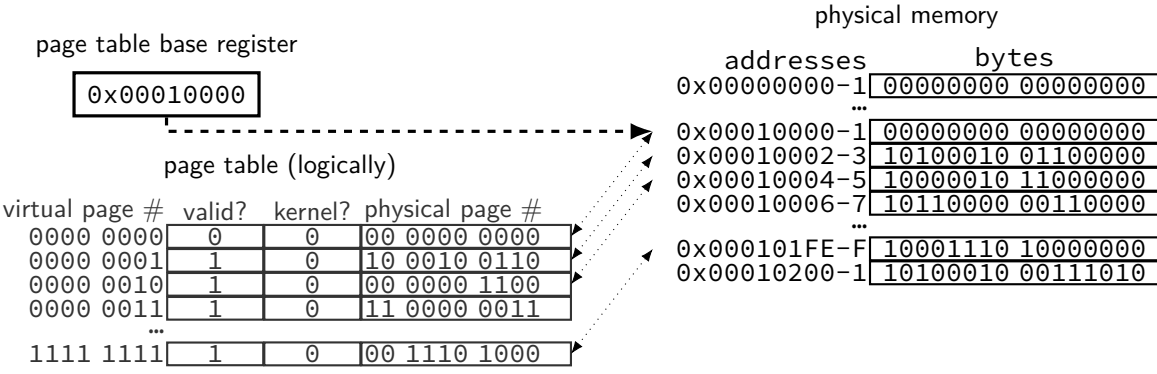
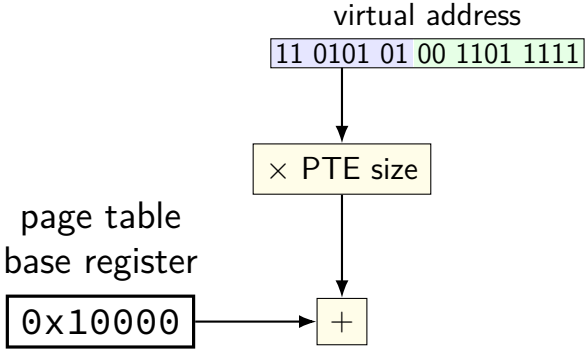


memory access with page table

virtual address

11 0101 01 00 1101 1111

memory access with page table



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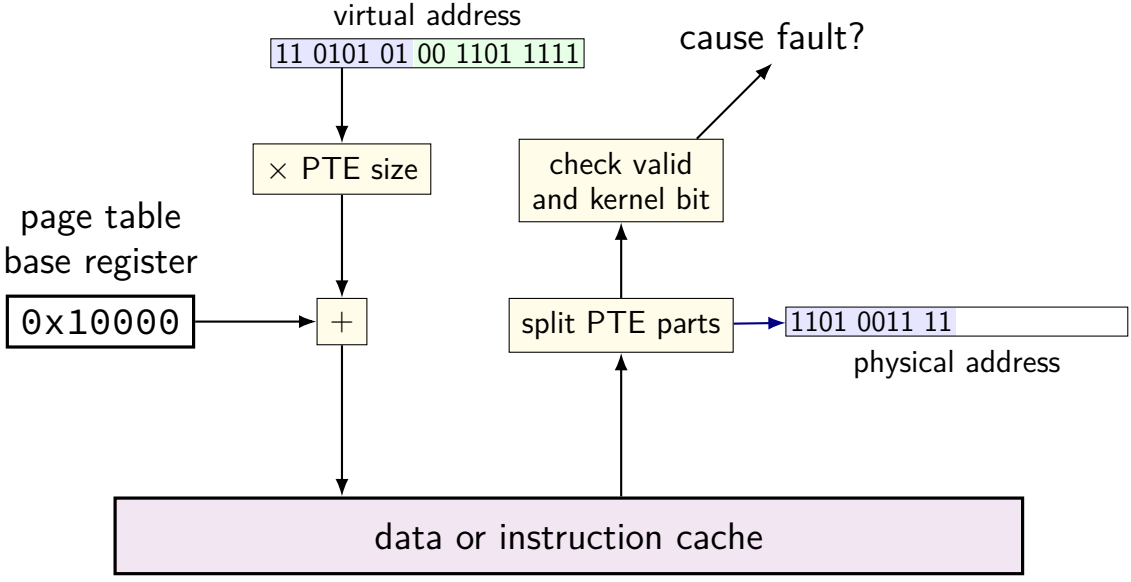
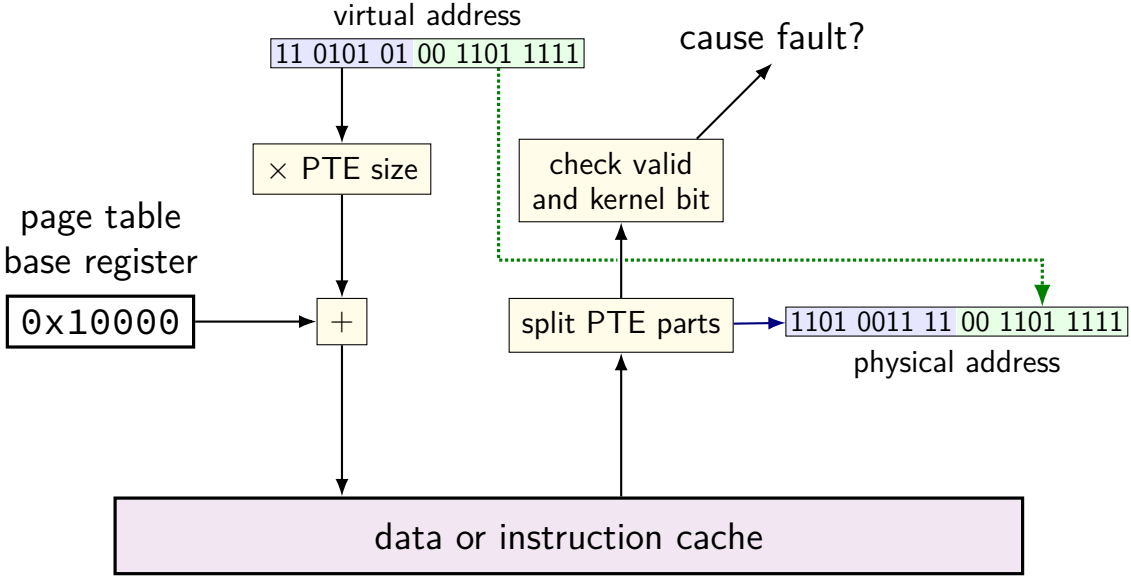
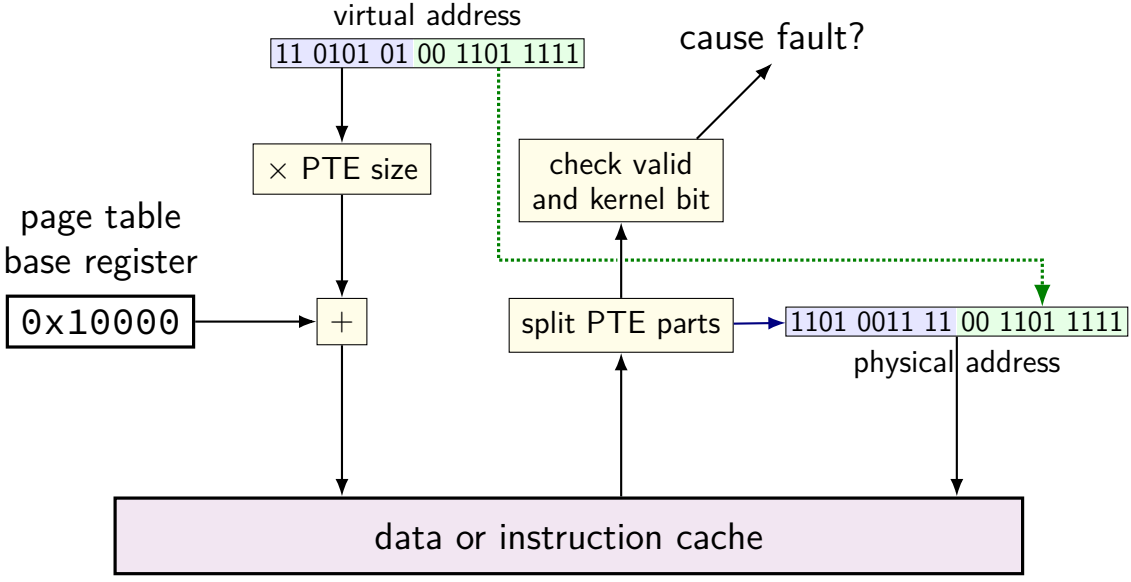


memory access with page table



memory access with page table



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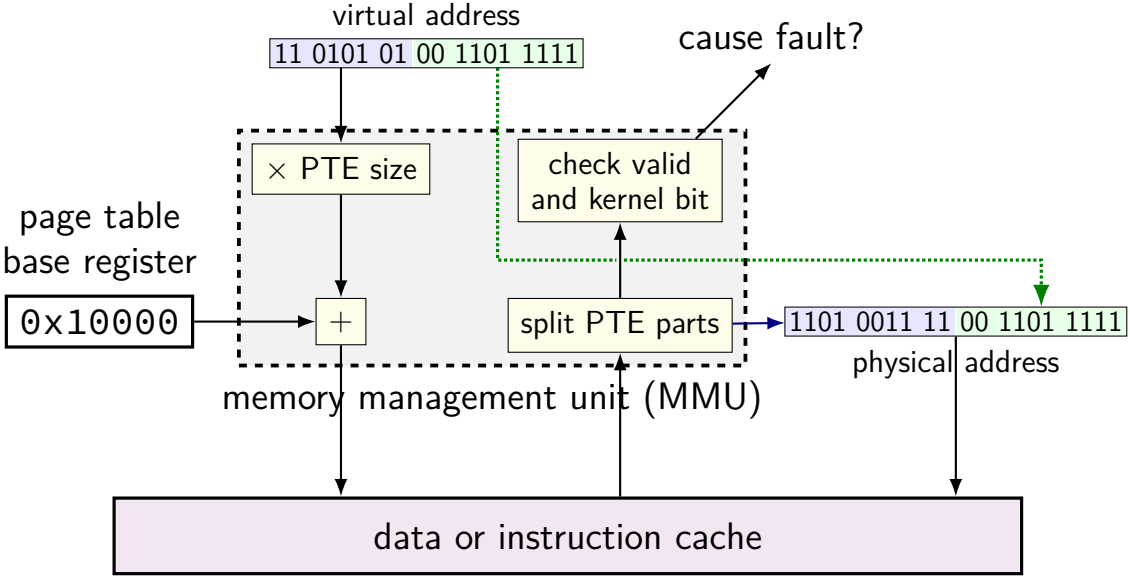

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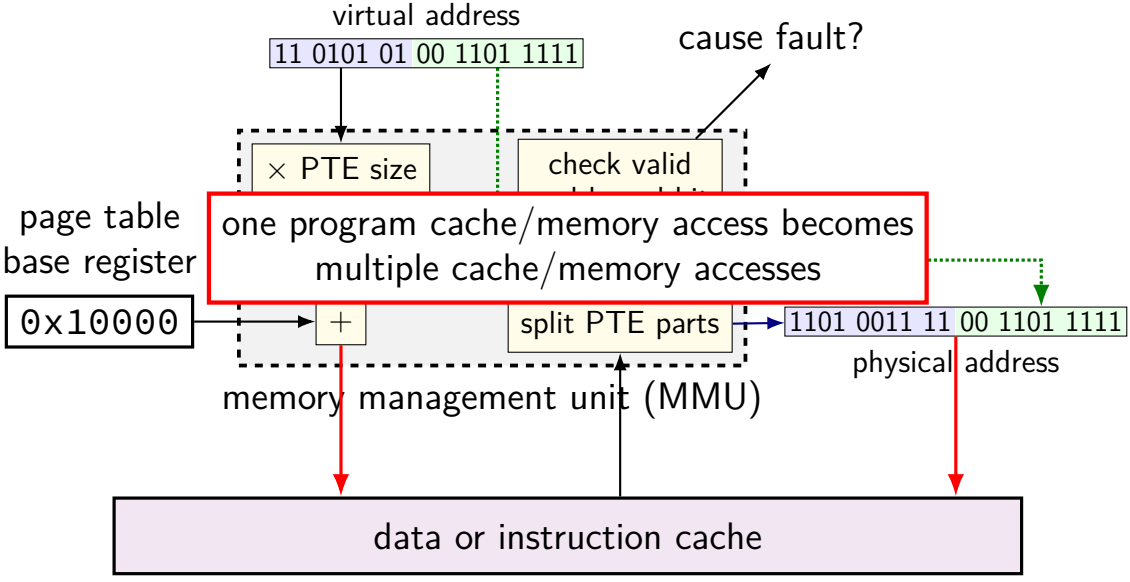

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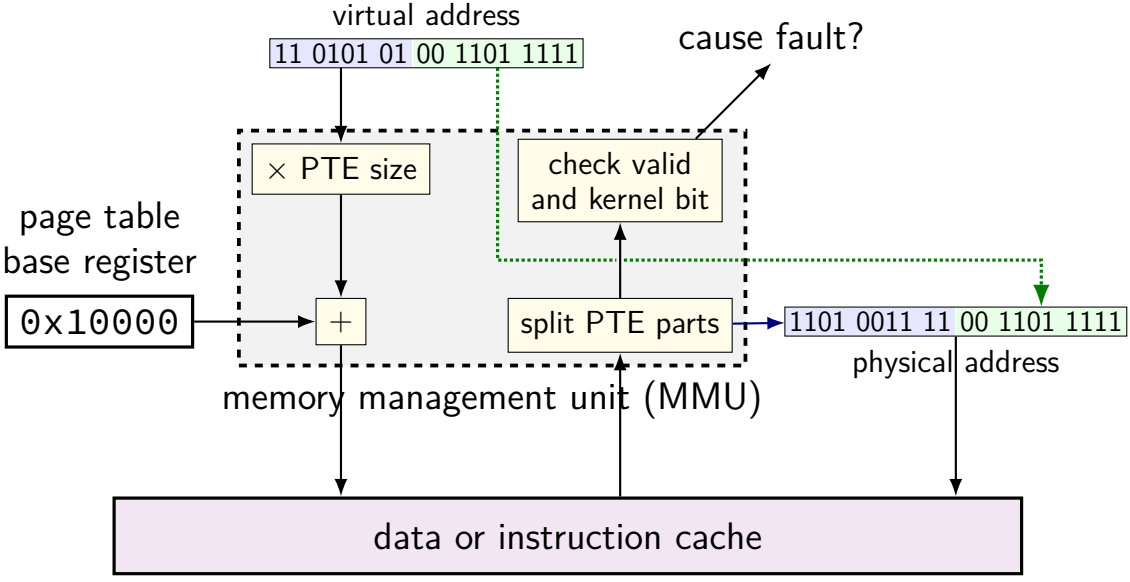
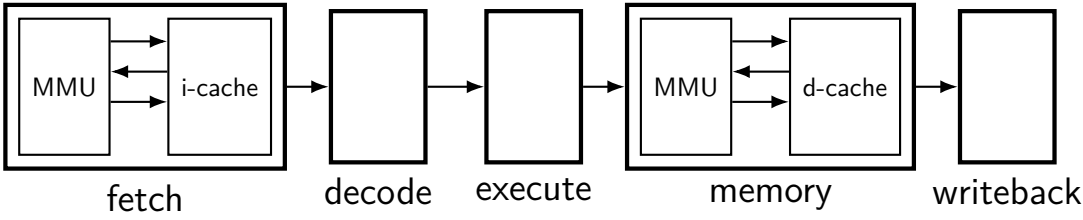


MMUs in the pipeline



up to four memory accesses per instruction

to make this fast — we use something like a cache (called a *TLB*) to avoid repeating recent lookups

exercise setup

5-bit virtual addresses, 6-bit physical addresses, 8-byte pages

page table

virtual page #	valid?	physical page #
00	1	010
01	1	111
10	0	000
11	1	000

physical addresses	bytes
0x00–3	00 11 22 33
0x04–7	44 55 66 77
0x08–B	88 99 AA BB
0x0C–F	CC DD EE FF
0x10–3	1A 2A 3A 4A
0x14–7	1B 2B 3B 4B
0x18–B	1C 2C 3C 4C
0x1C–F	1C 2C 3C 4C

physical addresses	bytes
0x20–3	D0 D1 D2 D3
0x24–7	D4 D5 D6 D7
0x28–B	89 9A AB BC
0x2C–F	CD DE EF F0
0x30–3	BA 0A BA 0A
0x34–7	CB 0B CB 0B
0x38–B	DC 0C DC 0C
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0x1C–F	1C 2C 3C 4C

phys. page 0

phys. page 1

physical addresses	bytes
	1 D2 D3
	5 D6 D7
	A AB BC
	E EF F0
0x30–3	BA 0A BA 0A
0x34–7	CB 0B CB 0B
0x38–B	DC 0C DC 0C
0x3C–F	EC 0C EC 0C

exercise

5-bit virtual addresses, 6-bit physical addresses, 8-byte pages

(virtual addresses) `0x18` = ???; `0x03` = ???; `0x0A` = ???; `0x13` = ???

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exercise

5-bit virtual addresses, 6-bit physical addresses, 8-byte pages

(virtual addresses) `0x18` = `00`; `0x03` = 0x4A; `0x0A` = ???; `0x13` = ???

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00	1	010
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10	0	000
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exercise

5-bit virtual addresses, 6-bit physical addresses, 8-byte pages

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1-level example

6-bit virtual addresses, 6-bit physical; 8 byte pages, 1 byte PTE

page tables 1 page; PTE: 3 bit PPN (MSB), 1 valid bit, 4 other bits;

page table base register `0x20`; translate virtual address `0x31`

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physical addresses	bytes
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0x34–7	CB 0B CB 0B
0x38–B	DC 0C DC 0C
0x3C–F	EC 0C EC 0C

0x31 = 11 0001

PTE addr:

0x20 + 6 ×1 = 0x26

PTE value:

0xF6 = 1111 0110

PPN 111, valid 1

M[111 001] = **M[**0x39]

→ 0x0C

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backup slides