CS 3330: Computer Architecture Spring 2019

Problem Set 3

HW Out: Tue, Apr. 2 **HW Due:** Mon, Apr. 15 *(40 points)*

HONOR PLEDGE:
On my honor as a student, I have neither given nor received unauthorized aid on this assignment/examination.

Signature: _____

Name: _____ Date: _____

Note: Answer each problem in the boxes provided. Any writing outside of the boxes will NOT be graded.

1. **Cache Performance (15 points)**.

   (a) **(5 points)** Doubling the L1 data cache size of a processor from 32KB to 64KB without changing its associativity reduced the L1 miss rate from 8% to 4%, for a given benchmark workload that has 20% loads and 5% stores. However, it was observed that this slowed down the workload by 3.2%. Quantitatively deduce what contributed to this slowdown. Assume that the L1 miss penalty is 20 cycles, and the original CPI was 1.25.

   (b) **(5 points)** By increasing the associativity of the L1 data cache, we were able to further reduce the miss rate to just 2%. Compute the performance impact on the given workload due to this change.

(c) **(5 points)** Would your answer to (b) change if the L1 cache was a unified cache? Show your work.

2. **Cache Policies (10 points).**

(a) **(5 points)** A classic inorder scalar processor employs a 32KB write-through write-allocate L1 data cache with a cache line size of 64 bytes, a miss rate of 5%, and a miss penalty of 20 cycles, for a given benchmark workload that has 20% loads and 5% stores. Compute the read and write bandwidth (number of bytes read/written per cycle) assuming no data and control hazards. Assume that we only have L1 data cache and main memory, and you are examining how much data moves between the L1 data cache and the main memory. So, for example, do not count traffic between the CPU and L1, just between L1 and memory. Also, assume that you always load and store quadwords.

(b) **(5 points)** Compute the read and write bandwidth assuming the cache described above is write-back and that 30% of the lines are marked dirty at any given point of time in execution.

3. **Cache Attacks (15 points).** Consider the following victim code.

```
double A[4096] = { ... };
int secret = ... ;
int res = 0;
for (i = 511; i >= 0; i--) {
    if (((secret >> i) & 0x1) == 1) {
        res ^= A[i * 8];
    } else {
        res ^= 2;
    }
}
```

(a) **(5 points)** If the above victim code ran on a processor with a 4-way set associative cache with 64-byte lines, how large should the cache be to avoid self conflicts between the elements of the array A? Show your work.

(b) **(6 points)** Assuming the cache organization computed in (a), find the minimum range of addresses in the eviction set of a PRIME+PROBE attacker if she only seeks to infer bit 500 (i = 500) of the secret key. Assume that the base address of the array A is 0x10000000 and the base address of the eviction set is 0x15000000.

(c) **(4 points)** Assuming the cache organization computed in (a), find the set of lines that a FLUSH+RELOAD attacker would flush if she only seeks to infer bits 8 through 15 (i = 8 to 15) of the secret key. Assume that the base address of the array A is 0x10000000 and that the array is shared between the attacker and the victim.