CS3330 Exam 2 – Spring 2014

Name: _____

Directions: Put the letter of your selection or the short answer requested in the box. Write clearly: if we are unsure what you wrote you will get a zero on that problem.

If you do not sign the pledge on the last page you will get a zero on the entire quiz.

. . . . . .

Question 1: Consider a two-stage pipeline: one stage has fetch and decode, the other has execute, memory, and writeback. Condition code information is available at the end of the execute phase and might be needed at the beginning of the fetch stage of the next instruction. Using data forwarding, the pipeline-introduced delay associated with a branch would be at most

A 0 cycles
B 1 cycle
C 2 cycles

Answer:

Question 2: Suppose we have an ALU that might take several cycles to process a single operation. The ALU has an output signal `busy` that is 1 if it needs another cycle with the same operation, 0 if it is ready for a new operation next cycle.

Consider a pipeline register earlier in the pipeline than the ALU. What best describes how that register should react to a 1 in the `busy` bit?

A stall
B it depends on if this is the first `busy` signal emitted by the ALU for this operation or not
C normal operation
D bubble

Answer:

Question 3: A pipeline register is currently emitting an `addl` instruction and is being given a bubble signal with an `xorl` instruction as its input. What will it emit next cycle?

A `addl`
B `xorl`
C `bubble`
D `stall`
E `nop`
F None of the above

Answer:

Question 4: Suppose we have an ALU that might take several cycles to process a single operation. The ALU has an output signal `busy` that is 1 if it needs another cycle with the same operation, 0 if it is ready for a new operation next cycle.

Consider a pipeline register several stages after the execute phase. What best describes how that register should react to a 1 in the `busy` bit?

A stall
B normal operation
C it depends on if this is the first busy for this operation or not
D bubble

Answer:

Question 5:

A 12-bit address *ABCDEFGHIJKL* (where each letter represents a single bit) is sent to a cache with 2 sets of 8 lines each; each block has 4 words of 1 byte each. What is the set index? (if you think it is the first three bits, you would answer *ABC*)

Answer:

Question 6: The I/O Bus connects the disk, USB, network card, and graphics card to which other computer component?

A Main Memory
B Schoolhouse
C CPU
D Bus Interface
E I/O Bridge

Answer:

Question 7: Select the most correct statement from the following as applied over the last two decades:

A Processors and memory both get faster, but processors get faster faster than memory does
B Memory gets faster but processors do not
C Processors and memory both get faster, but memory gets faster faster than processors do
D Processors get faster but memory does not

Answer:

Question 8: A fully-associative cache is like a

A direct-mapped cache with only one set
B direct-mapped cache with only one line per set
C set-associative cache with only one line per set
D set-associative cache with only one set

Answer:

Question 9: A pipeline register is currently emitting an `addl` instruction and is being given neither a bubble nor a stall signal, with an `xorl` instruction as its input. What code does it emit next cycle?

A `addl`
B `xorl`
C `nop`
D `bubble`
E `stall`
F None of the above

Answer:

Question 10:

A write-_____ cache immediately forwards writes to the next larger cache. (write your answer in the box)

Answer:

Question 11: Consider the following code:

```
void f(int** a, int**b, unsigned n, unsigned m) {
     for(i = 0; i+1 < n; i += 1)
         for(j = m-1; j >= 0; j -= 1)
             a[m-1-j][i] = b[j][i] * b[j][i+1];
 }
```

Which of the following changes would make the largest positive impact on its cache locality?

A Block the accesses by nesting three or four for loops instead of just two
B Change `int**` to `int*`
C Change the for-j loop to count up from `0`, not down from `m-1`
D Put the for-i loop inside of the for-j loop instead of the other way around

Answer:

Question 12: Your code multiplies each element of a large array by 2. Your array accesses can benefit from

A spatial locality
B temporal locality
C both of the above
D none of the above

Answer:

Question 13: Consider the following code:

```
void f(int** a, int**b, unsigned n, unsigned m) {
     for(i = 0; i < n; i += 1)
         for(j = m-1; j >= 0; j -= 1)
             a[i][j] = b[j][i];
 }
```

Which of the following changes would make the largest positive impact on its cache locality?

A Change `int**` to `int*`
B Put the for-i loop inside of the for-j loop instead of the other way around
C Change the for-j loop to count up from `0`, not down from `m-1`
D Block the accesses by nesting three or four for loops instead of just two

Answer:

Question 14: Pipelining generally

A reduces throughput and reduces latency
B increases throughput and reduces latency
C increases throughput and increases latency
D reduces throughput and increases latency

Answer:

Question 15: Suppose addresses A and B both map to the same line of a direct-mapped cache but with different tags. Code reads A once then reads B once. The read of B is a

A capacity miss
B conflict miss
C hit
D cold miss

Answer:

Question 16: Consider a longer pipeline: F, D, E, Mr, Mw, W, where memory read and memory write have been split into two phases to facilitate memory-memory moves. Data needed in the E phase is always from a register, and new register values can can appear in the D, E, or Mr phases. If we have data forwarding, what is the largest data dependency delay we could see?

A 3 cycles
B no delay
C 4 cycles
D 5 cycles
E 6 or more cycles
F 1 cycle
G 2 cycles

Answer:

Question 17: Starting from a cold cache, your program accesses one byte at a time in order from address 0x000 to address 0x100, then terminates. Which of the following characteristics of the cache will help the program run faster? (pick all that apply)

A large blocks
B more sets
C small blocks
D more lines per set
E none of the above will help

Answer:

Question 18: Suppose addresses A and B both map to the same line of a set-associative cache but with different tags. Code reads A, then B, then A, then B. The second read of B is a

A cold miss
B hit
C capacity miss
D conflict miss

Answer:

Question 19: What is the main reason to have separate instruction and data caches?

A you don't usually access code as data so you won't get many extra hits if you merged them
B they are on separate memory chips so they have to have separate caches
C each core should have its own instruction cache but they all share one data cache
D access patterns are different so different cache organisations (set size, etc) make sense.
E you don't want your data and cache accesses to conflict with one another

Answer:

Question 20:

A 10-bit address is sent to a cache with 8 sets of 2 lines; each block has 2 words of 4 bytes each. How many bits long is the tag?

Answer:

Question 21: A pipeline register is currently emitting an `addl` instruction and is being given a stall signal with an `xorl` instruction as its input. What code does it emit next cycle?

A `nop`
B `addl`
C `stall`
D `bubble`
E `xorl`
F None of the above

Answer:

Question 22: Suppose we have an ALU that might take several cycles to process a single operation. The ALU has an output signal `busy` that is 1 if it needs another cycle with the same operation, 0 if it is ready for a new operation next cycle.

Consider the pipeline register at the end of the execute phase. What best describes how that register should react to a 1 in the `busy` bit?

A it depends on if this is the first `busy` signal emitted by the ALU for this operation or not
B stall
C bubble
D normal operation

Answer:

Question 23:

When a dependency has the potential to cause incorrect computation in a pipeline, it is called a _____ (write your answer in the box).

Answer:

Question 24: Your code intentionally keeps addresses far from one another to foil certain kinds of security vulnerabilities. Your data accesses can benefit from

A temporal locality
B spatial locality
C both of the above
D none of the above

Answer:

Question 25: Organize the following kinds of storage from fastest to slowest. Do this by writing four letters in order in the box.

A Magnetic disk
B SRAM
C Solid-state disk
D DRAM

Answer:

Pledge:

On my honor as a student, I have neither given nor received aid on this exam.

_____

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