CS 3330 Exam 1 – Fall 2016

Name: EXAM KEY **Computing ID:** KEY

Letters go in the boxes unless otherwise specified (e.g., for **C** 8 write "C" not "8").
Write Letters clearly: if we are unsure of what you wrote you will get a zero on that problem.
Bubble and Pledge the exam or you will lose points.
Assume unless otherwise specified:

- little-endian 64-bit architecture
- `%rsp` points to the most recently pushed value, not to the next unused stack address.
- questions are single-selection unless identified as select-all

Variable Weight: point values per question are marked in square brackets.
Mark clarifications: If you need to clarify an answer, do so, and also add a * to the top right corner of your answer box.

Information for questions 1–2
Y86-64 has 12 `icodes`: `halt`, `nop`, `rrmovq`, `irmovq`, `rmmovq`, `mrmovq`, `OPq`, `jXX`, `pushq`, `popq`, `call`, and `ret`. The following questions should be answered with the number of those 12 that have the listed property. Valid answers range from 0 to 12.

Question 1 [2 pt]: (see above) How many set the condition codes?

Answer: 1 – half credit for 2, quarter credit for 3

Question 2 [2 pt]: (see above) How many perform math in the execute stage? (The textbook said some instructions always add 0 to something (e.g., valE = 0 + valC); don't include that 0+ addition as "math" for this question.)

Answer: 7 – half-credit for 5 or 3

Question 3 [2 pt]: The following are true of memory layout in x86-64 Linux. Which one is due to the x86-64 ISA?

A the stack grows towards smaller addresses
B the top of the address space is used by the OS
C the bottom of the address space is unused
D the heap grows toward larger addresses
E executable code begins at address 0x40000000

Answer: A

Information for questions 4–5
Consider the following Y86-64 assembly program and its corresponding encoding. (On the left-most column is the memory address of each instruction, followed by its encoding, listed as a sequence of bytes in hexadecimal.)

Assume the program register r8 contains the value 0xA before the given assembly is run.

```
0x000: 30 f0 0a 00 00 00 00 00 00 00 |         irmovq label, %rax
0x00a: 50 08 00 00 00 00 00 00 00 00 | label:  mrmovq 0(%r8), %rax
```

Question 4 [2 pt]: (see above) What is the value of `%rax` after the first instruction (the `irmovq`) executes?

A the machine will stop with the invalid address (`STAT_ADR`) status
B 0xC
C 0x5008000000000000 (ends with 12 zeroes)
D 0x0
E 0xA
F 0x850
G 0x5

Answer: E

Question 5 [2 pt]: (see above) What is the value of `%rax` after the second instruction (the `mrmovq`) executes?

A the machine will stop with the invalid address (`STAT_ADR`) status
B 0x8
C 0x30f00a0000000000 (ends with 10 zeroes)
D 0x850
E 0x30
F 0xA
G 0x0
H 0xaf030
I 0x5008000000000000 (ends with 12 zeroes)

Answer: D

Question 6 [2 pt]: Suppose that `x` is the `signed char` containing the value -33 (0b11011111) and `unsigned char y = (unsigned char)x;`. Which of the following are true?
Select all that apply

A `x == (int)x`
B `x == y` not true because implicitly become int before comparing
C `(x >> 1) < x` arithmatic
D `(y >> 1) < y` logical

Answer: A D

Information for questions 7–8
The following ask about wiring of the SEQ processor.

Question 7 [2 pt]: (see above) The **instruction memory** has one input and one output. During a cycle in which we execute `call` instruction, the value of the input should be set to:

A the address of the call instruction
B the output of the data memory
C the immediate value (target address) contained within the call instruction
D the address of the instruction following the call instruction in memory
E the output of the ALU
F none of the above

Answer: A

Question 8 [2 pt]: (see above) The **program counter register** has one input and one output. During a cycle in which we execute `call` instruction, the value of the input should be set to:

A the address of the call instruction
B the output of the data memory
C the immediate value (target address) contained within the call instruction
D the output of the ALU
E the address of the instruction following the call instruction in memory
F none of the above

Answer: C

Question 9 [2 pt]: Choose the correct compilation of `rax = (rbx ? rcx : rdx)` Due to a typo, this question was not graded

A

```
    andq %rbx, %rbx;
    jne p2;
    rrmovq %rdx, %rax;
p2: rrmovq %rcx, %rax
```

B

```
    andq %rbx, %rbx;
    rrmovq %rdx, %rax;
    je p2;
    rrmovq %rcx, %rax
p2:
```

C

```
    andq %rbx, %rbx;
    je p2;
    rrmovq %rdx, %rax;
p2: rrmovq %rcx, %rax
```

D

```
    andq %rbx, %rbx;
    rrmovq %rdx, %rax;
    jne p2;
    rrmovq %rcx, %rax
p2:
```

Answer: B

Question 10 [2 pt]: If we extend Y86-64 to include a new instruction mr*OP*q which is like *OP*q except that it allows for a memory source (e.g., `mrxorq 33(%r11), %r12`), how long would its encoding be?

A 1 byte
B 2 bytes
C 10 bytes
D 9 bytes
E none of the above

Answer: C

Question 11 [2 pt]: What is $log_2(32G)$? Answer as a normal base-10 number.

"Memorizing powers of two became so important later in the semester. (I neglected to memorize them until I needed them later and I regret it.)" —a TA

Answer: 35 – half for 3_, half for _5

Information for questions 12–13
Recall that we use two condition code flags: SF (the sign flag) is 1 for a negative number and ZF (the zero flag) is 1 for the value zero.

Question 12 [2 pt]: (see above) After executing the Y86-64 assembly instruction `xorq %rax, %rax`, what are possible values for the condition code bits SF and ZF?
Select all that apply.

A ZF = 1, SF = 0
B ZF = 0, SF = 1
C ZF = 1, SF = 1
D ZF = 0, SF = 0

Answer: A

Question 13 [2 pt]: (see above) After executing the Y86-64 assembly instruction `andq %rax, %rax`, what are possible values for the condition code bits SF and ZF?
Select all that apply.

A ZF = 1, SF = 0
B ZF = 0, SF = 1
C ZF = 0, SF = 0
D ZF = 1, SF = 1

Answer: A B C

Information for questions 14–15
In lab you coded with three kinds of lists: sentinel-terminated arrays; length arrays (also called vectors or ranges); and linked lists.

Question 14 [2 pt]: (see above) Which requires the **least** new memory to be allocated to extend a 64-element list to have a 65th element? Assume we use `malloc` to allocate any new memory needed.

A sentinel-terminated arrays
B linked lists
C length arrays (also called vectors or ranges)

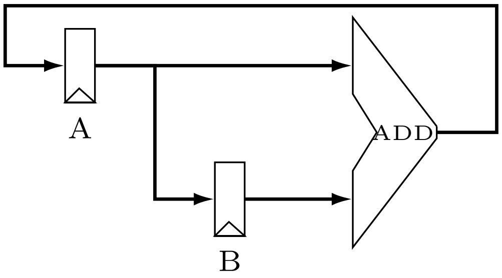
Answer: B

Question 15 [2 pt]: (see above) Assume we have 8-byte pointers and list elements are 1-byte values. Which type of list uses the **most** memory?

A length arrays (also called vectors or ranges)
B sentinel-terminated arrays
C linked lists

Answer: C

Question 16 [2 pt]:



Answer: 5 (half credit for 8, quarter for 3)

Consider the above circuit, which contains two registers and a ALU that only adds its operands. If register A and register B initially output 1, what value will register A output after 3 rising clock edges happen?

Question 17 [3 pt]: What are the possible return values of the following C function?

```
int foo(int x) {
  int y;
  do {
    y = x;
    x = x >> 1;
  } while (x != y);
  return x;
}
```

Select all that apply.

A MAX_INT (the most positive possible int)
B a value not listed above
C MIN_INT (the most negative possible int)
D 0
E -1
F 1

Answer: D E

Question 18 [2 pt]: What does the following C code return?

```
       int x = 2, y = 2;
       if (x) goto qux;
       x -= y;
qux:   if (!x) goto plugh;
       y -= 1;
       if (y >= x) goto qux;
plugh: return (10*x + y);
```

Answer as either a normal base-10 number or with one of the words “error” (if it contains an error) or “loops” (if it runs forever).

Answer: 21

Question 19 [2 pt]: Which of the following is more typical of RISC than CISC?

A addressing is simplified so that memory operands may appear in any instruction
B common tasks like pushing onto the stack are reduced to a single instruction
C all instructions are simplified to have the same encoded length
D all of the above
E none of the above

Answer: C

Information for questions 20–20
Assume that `x` and `y` are 32-bit `int`-type variables in C. Assume that their initial values are positive (strictly greater than 0).

Question 20 [8 pt]: (see above) Which of the following are guaranteed to be true?

*Note: this will be graded like 8 true/false questions; answer by putting a **check-mark** in the true boxes and leaving the false ones **blank**.*

Select all that apply

A ☑ `(x|y) >= (x&y)`

B □ `(x+y) - ((x&y)<<1) >= (x&y)`

C ☑ `~y < -y`

D □ `(x>y ? x+~y : y+~x) >= 0`

E □ `((-x)>>2) == (-(x>>2))`

F □ `x|~y == -1` due to a typo, this question was not graded

G ☑ `x|~x == -1`

H ☑ `x^-y < 0`

Question 21 [2 pt]: Which of the following only occur on a rising clock edge?
Select all that apply

A register file read
B data memory write
C data memory read
D register file write

Answer: B D

Pledge:

On my honor as a student, I have neither given nor received aid on this exam.

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