NEW ULTRA HIGH DENSITY EPROM AND FLASH EEPROM WITH NAND STRUCTURE CELL

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ABSTRACT

In order to realize ultra high density EPROM and Flash EEPROM, a NAND structure cell is proposed. This new structure is able to shrink cell size without scaling of device dimensions. The NAND structure cell realizes a cell as small as 6.43 um^2 using 1.0 um design rule. As a result, cell area per bit can be reduced by 30% compared with that of a 4M bit EPROM using the conventional structure and the same design rule. It is confirmed that each bit in a NAND cell is able to be programmed selectively. This high performance NAND structure cell is applicable to high density nonvolatile memories as large as 8M bit EPROM and Flash-EEPROM or beyond.

INTRODUCTION

With the development of VLSI technologies, bit density of nonvolatile memories is undergoing revolutionary growth. To realize Megabit density memories, current EPROM's have been simply shrunk by introducing self-aligned floating gate structure and scaled dielectric. However, the current EPROM cell is now beginning to reach limitation in the scaling law, because it is hard to reduce contact hole size and spacing between gate electrode and drain contact hole. Therefore, a new NAND structure cell is proposed to extend memory density beyond Megabit level. The cell described in this paper realizes 30% cell area reduction compared with a current approach, such as contact hole size reduction. This NAND structure cell is able to be fabricated by current EPROM process technology.

This paper describes the structure, operation principle and reliability of a new NAND structure cell.

MEMORY CELL ARRAY

The new NAND structure cell is fabricated by conventional double poly silicon technology. The floating gate is made of the first poly-Si layer, and the control gate is made of the second poly-Si layer. The gate length of memory cell transistor is 0.9 um. The gate oxide thickness under the floating gate is 200A. The interpoly oxide between the floating gate and the control gate is also 200A thick. These parameters are the same in 4M bit EPROM of conventional technology [1]. The new NAND structure cell having 4 bits is shown in Fig.1-(a) compared with the current EPROM cell having 4bits as shown in Fig.1-(c). The NAND cell arranges each bit in series. The equivalent circuit of the NAND cell is shown in Fig.1-(b). Figure 2 shows occupied area of each bit versus number of bits connected in one NAND cell structure. The current EPROM cell has one contact area per two bits. However, for a new NAND cell , only single contact hole is required per two NAND cells. As a result, the NAND cell can realize smaller cell area per bit than the current EPROM cell.

PRINCIPLE OF OPERATION

The NAND structure cell is able to be programmed by hot electron injection to the floating gate and erased by UV irradiation or electric field emission of electrons from the floating gate. In a program mode, 9V is applied to the bit line. 10V is applied to the word line of the selected bit and 20V is applied to the other three word lines of unselected bits in the NAND structure cell. The bit line voltage is mostly supplied between the

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drain and source of the selected bit. Therefore, the selected bit operates in saturation mode and hot electrons are generated in the channel. On the contrary, the other three unselected bits operate in deep triode mode because of high gate voltage, where the hot electrons are not generated. Therefore, it is possible to write only the selected bit in the NAND cell . Figure 3 shows that an EPROM has not been written in the triode operation mode. This programming characteristics were measured by the following conditions. Two resistors of 6k-ohms are connected between V_{pp} and drain and also between V_{ss} and source. The resistance of both resistors is equivalent to the sum of that of the channels and the diffusion layers of the rest bits in the NAND cell. The threshold voltage shift of a written transistor strongly depends on the control gate voltage during programming. The threshold voltage shift does not occur with V_{cg} exceeding 13V.

In a reading operation, 1V is applied to bit lines, the low level voltage is applied to the selected word line and the high level voltage is applied to the other unselected word lines in the NAND cell. Then the selected bit flows current when the bit is in erased state and does not flow current when it is in written state.

EXPERIMENTAL RESULTS

PROGRAMMING:

The programming characteristics of the NAND cell are shown in Figs.4, 5 and 6. Figure 4 shows the threshold shifts of the selected bit and the other three unselected bits as a function of the programming time with all bits in the NAND cell in erased state by UV irradiation. The selected bit is written and the other three unselected bits are not written. Figure 5 also shows the threshold shifts as a function of programming time with the selected bit in erased state by UV irradiation and the other three unselected bits in written state. It is shown that the selected bit is written with the threshold voltage of the other three unselected bits remaining at the initial value. After sequential programming of the NAND cell, the threshold windows are kept at lager than 2V, as shown in fig.6.

READING:

Figure 7 shows sensing drain currents in the read out mode of a NAND cell as a function of bit line voltage. 4V is applied to the control gate of the addressed bit and 7V is applied to the control gates of the other bits. Current does not flow at all when the addressed bit is in written state. On the other hand, current increases as the drain voltage increases when the selected bit is in erased state.

RELIABILITY:

Read retention characteristics is shown in Fig.10. No threshold shift during read operation in any bit of the NAND cell has been observed.

Data retention of the NAND cell is the same as that of current EPROM, because each bit of the NAND cell has the same structure as that of current EPROM cell.

CONCLUSION

A new EPROM with the NAND structure cell has been developed. Each bit of the NAND cell can be programmed and read separately, and also the reliability of the new NAND structure is excellent as same as the current EPROM.

This new technology enables one to shrink the cell size by 30% as compared with current EPROMs without scaling the device dimensions. Flash-EEPROM using NAND cell array is also realized by adding an extra erase gate. This NAND structure can be successfully applied 8M or 16M bit EPROMs and Flash-EEPROMs.

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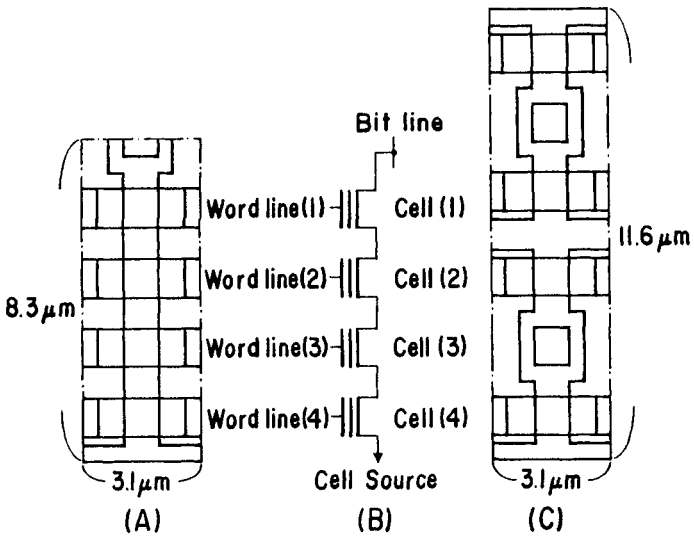

Fig.1. Comparison between a new NAND structure cell (A) and conventional cell (C). Figure (B) shows equivalent circuit of the NAND structure cell having 4 bits.

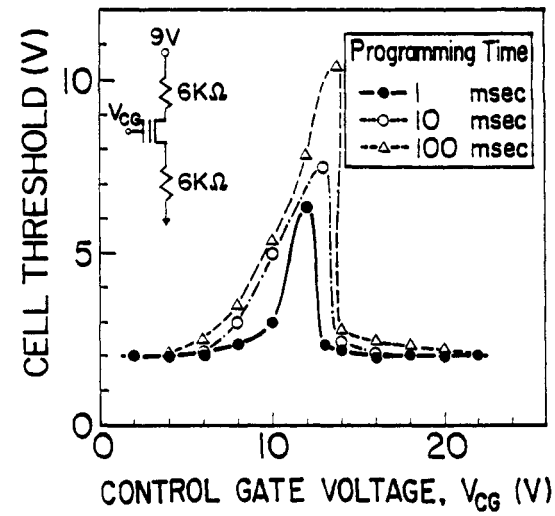

Fig.3. Cell threshold voltage as a function of a control gate voltage.

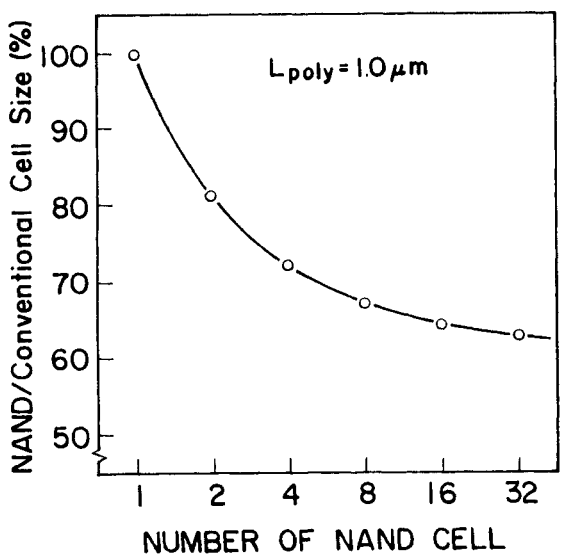

Fig.2. Occupied area of each bit as a function of the number of bits connected in one NAND structure cell.

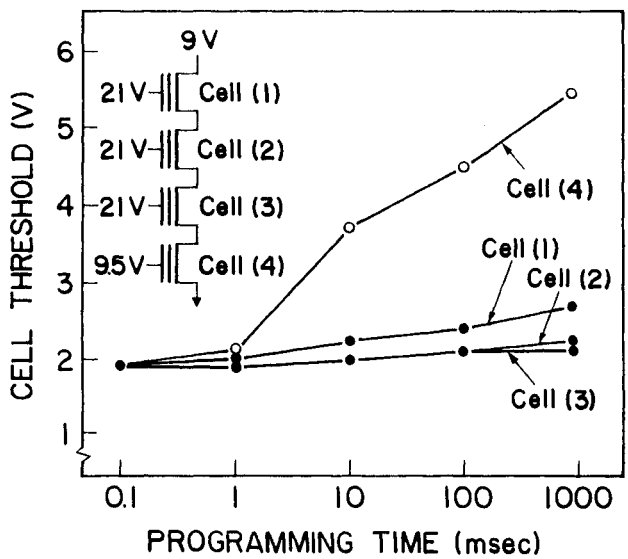

Fig.4. Cell threshold voltage as a function of programming time in the NAND structure cell. All bits are erased by UV initially, then cell(4) is programmed selectively.

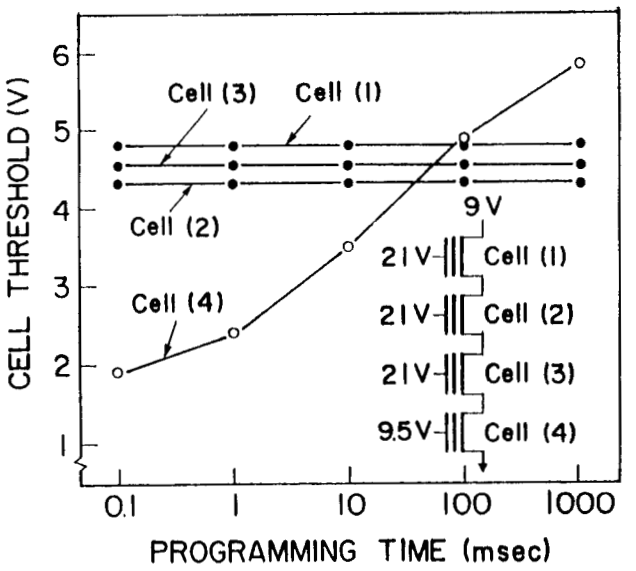

Fig.5. Cell threshold voltage as a function of programming time in the NAND structure cell. Cell(1), (2) and (3) are programmed and cell(4) is erased by UV initially, then cell(4) is programmed selectively.

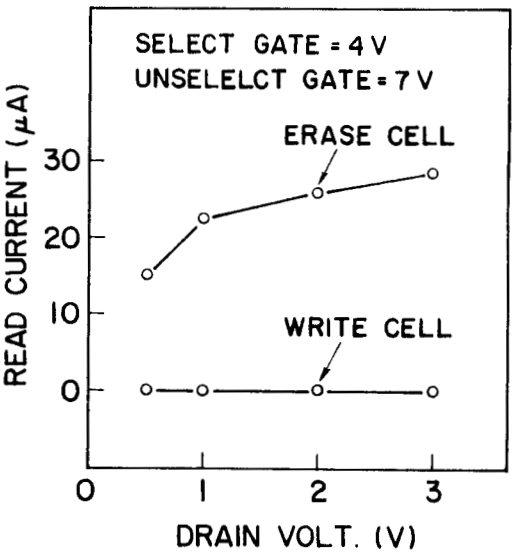

Fig.7. Cell current as a function of a drain voltage.

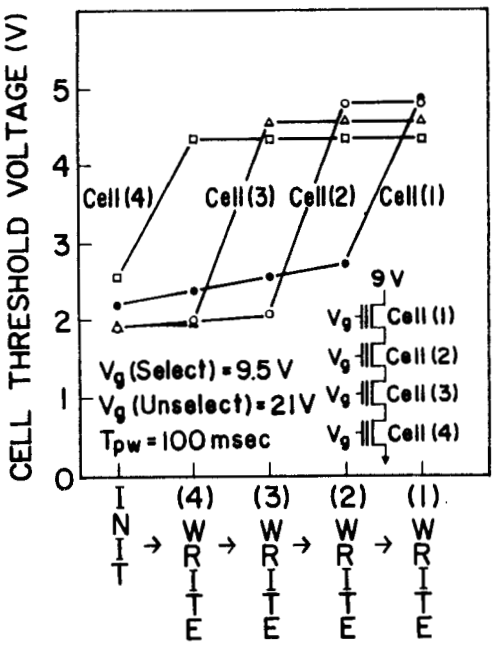

Fig.6. NAND cell threshold voltage after sequential programming from cell(4) to cell(1).

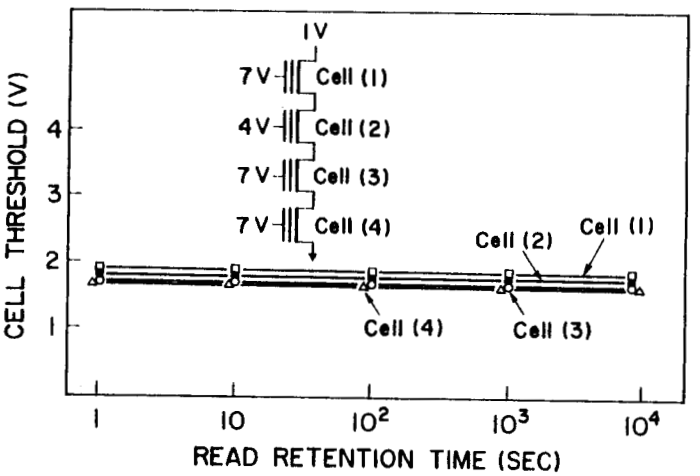

Fig.8 Read retention characteristcs.