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## COA1 Exam 1 - Fall 2019

Name: $\qquad$ Computing ID: $\qquad$
Write Letters clearly: if we are unsure of what you wrote you will get a zero on that problem. Bubble and Pledge the exam or you will lose points.
Single-select by default: Multiple select are all clearly marked; answer them by putting 1 or more letters in the box, or writing "none" if none should be selected.
Page-at-a-time Grading: We scan your exam and grade each page separately. Do not refer to other pages, scrratch paper, etc., in your answer.
Mark clarifications: If you need to clarify an answer, do so, and also add a $\star$ to the top right corner of your answer box.

Question $1[\mathbf{2 p t}]:$ What is $0 \times 3 \mathrm{D}$ in decimal?


## Information for questions 3-4

The following assume 8 -bit 2 's-complement numbers. For each number, bit 0 is the low-order bit, bit 7 is the high-order bit.

Question $3[\mathbf{2 p t}]$ : (see above) Complete the following sum, showing your work (carry bits, etc)

```
    1 1 0 0 0 1 0 0
+ 1 0 0 1 1 1 1 0
```

Question $4[\mathbf{2} \mathbf{p t}]$ : (see above) We call it overflow if the correct mathematical answer cannot fit in the available bits. Which of the following can experience overflow?
Select all that apply by putting 1 or more letters in the box.
A positive + positive
B positive + negative
C negative + positive
Answer:

Question 5 [ $\mathbf{4} \mathbf{~ p t}]$ : Draw a 4-input adder for single-bit values: that is, a set of logic gates with 4 input wires (no need to name them) each representing a number between 0 and 1 and a multi-bit
 the number of wires needed for this task). The gates should ensure that $z=$ the sum of all four inputs.
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Question 6 [ $\mathbf{2 ~ p t}]$ : A normalized floating-point number is positive if
A the high-order bit is 0
B the high-order bit is 1
C the high-order bit of the exponent is 0
D the high-order bit of the exponent is 1
E the exponent is not 0
F the high-order bit of the fraction is 0
Answer:

G the high-order bit of the exponent is 1
H the fraction is not 0

## Information for questions 7-9

Each question gives two expressions of 32 -bit two's-compliment integers $x$ and $y$. If the two are equivalent for all x and y , write "same"; otherwise, write an example x (and y if used in the expressions) for which the two are different.

Question 7 [ $\mathbf{2 ~ p t}$ ]: (see above)
$x^{\wedge} y \wedge x$ and $x+y-x$

Question 8 [2 pt]: (see above)
$x+y$ and $(x \& y)+(x \mid y)$

Question 9 [2 pt]: (see above)
( $\mathrm{x} \& 0 \times \mathrm{F} 0000000$ ) $\mid(\mathrm{x} \gg 4)$ and ( $\mathrm{x} \gg 4$ ) (that's an F followed by seven 0 s)
$\qquad$

Question 10 [ $\mathbf{2} \mathbf{~ p t ] : ~ W e ~ d i s c u s s e d ~ r e g i s t e r s ~ a s ~ a ~ k e y ~ c o m p o n e n t ~ o f ~ c i r c u i t s ~ a n d ~ t h e ~ o n l y ~}$ component that uses a clock. The clock is used to
A enable storage of values
B limit when changed input is remembered in storage
C decide when stored values become visible in output
D control when circuits can access stored values

| Answer: |
| :--- |
|  |

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## Information for questions 11-12

Suppose we extended the ISA simulator you wrote in Lab 03 with the following code:

```
if (reserved == 1 && icode == 3) {
    M[R[a]] = M[R[b]];
    return oldPC + ____;
}
```

Question 11 [ $\mathbf{2 p t} \mathbf{~ p t : ~ ( s e e ~ a b o v e ) ~ W h a t ~ n u m b e r ~ s h o u l d ~ b e ~ p l a c e d ~ i n ~ t h e ~}$ return statement where the code above has ____?

Answer:

Question 12 [ $\mathbf{2} \mathbf{~ p t}]$ : (see above) Using the new instruction, write a program that moves a byte from memory at address $r_{2}$ to memory at address $r_{1}$. Answer in hexadecimal bytes, separated by spaces.

Answer: $\qquad$

Information for questions 13-14
Suppose an array of two 32 -bit values ([0xabcdef01, $0 \times 7645231]$ ) is stored at address $0 \times 200$. What byte is stored at address $0 \times 204$ ? Answer in hexadecimal.

Question 13 [ $\mathbf{2} \mathbf{~ p t}]$ : (see above) Assume little-endian storage.

Question 14 [ $\mathbf{1} \mathbf{~ p t ] : ~ ( s e e ~ a b o v e ) ~ A s s u m e ~ b i g - e n d i a n ~ s t o r a g e . ~}$


Question 15 [ $\mathbf{2} \mathbf{~ p t}]$ : Why might an ethical engineer put a back-door in processor or software product?
Select all that apply by putting 1 or more letters in the box.
A for debugging
B to advanced remote support
C because the client isn't trustworthy
D by mistake (they're hard to avoid)
E because management insisted on it
Answer:
$\qquad$

Question 16 [ $\mathbf{2 ~ p t}]$ : Copyrights can protect a description of an ISA, but not the ISA itself. If ISAs are considered to be inventions, patents could protect them, preventing others for using the same ISA (without paying royalties) until the patent expires (typically after 20 years).

Opinions about the patentability of ISAs are varied. Provide one reason for and one reason against the patentability of an ISA. Note that "I want free computers" is not a sufficient reason against...

Pro-patent: $\qquad$
$\qquad$
$\qquad$
$\qquad$
Anti-patent: $\qquad$
$\qquad$
$\qquad$
$\qquad$

## Pledge:

On my honor as a student, I have neither given nor received aid on this exam. I will not discuss the content of this exam, even in vague terms, with anyone other than current course staff, until Friday 4 October 2019.

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## Our Example ISA

## Instruction Breakdown

Treat each instruction's first byte as having four parts:

| bits | name | meaning |
| :---: | :---: | :--- |
| 7 | reserved | If set, this instruction is reserved for future definition. |
| $[4,7)$ | icode | Specifies what action to take |
| $[2,4)$ | a | The index of a register |
| $[0,2)$ | b | The index of another register, or details about icode |

Some instructions use additional bytes, described below as "memory at pc + 1" or the like.

## Instructions

If reserved is 0 , consult the table below. In it, $r A$ means "the value stored in register number $a$ " and $r \mathrm{~B}$ means "the value stored in register number b ."

| icode | b | Behavior | add to pc |
| :---: | :---: | :---: | :---: |
| 0 | any | $r A=r B$ | 1 |
| 1 | any | $r A+=r B$ | 1 |
| 2 | any | $r A \&=r B$ | 1 |
| 3 | any | $r A=r e a d$ from memory at address $r B$ | 1 |
| 4 | any | write $r A$ to memory at address $r B$ | 1 |
| 5 | 0 | $r A=\sim r A$ | 1 |
| 5 | 1 | $r A=-r A$ | 1 |
| 5 | 2 | $r A=!r A$ | 1 |
| 5 | 3 | $r A=p c$ | 1 |
| 6 | 0 |  | 2 |
| 6 | 1 | $r A+=r e a d$ from memory at $p c+1$ | 2 |
| 6 | 2 | $r A \&=$ read from memory at $p c+1$ | 2 |
| 6 | 3 | $r \mathrm{~A}=\mathrm{read}$ from memory at the address stored at $\mathrm{pc}+1$ | 2 |
| 7 | any | if $r A<=0$, set $p c=r B$ | N/A |
| 7 | any | if $r$ A $>0$, do nothing | 1 |

If reserved is 1 , the above table does not define what the instruction means, but some other source (such as a question on this exam) might. If it has no defined meaning either here or elsewhere, leave the pc and all other registers and memory values unchanged.


[^0]:    Your signature here

