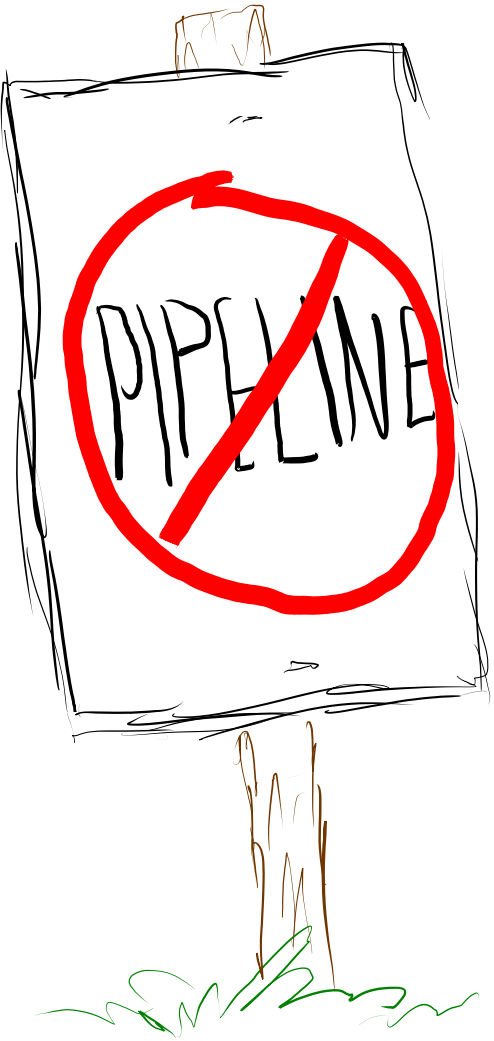
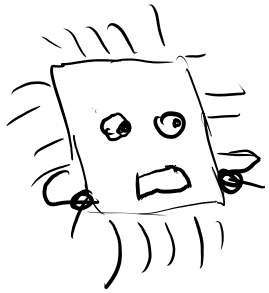
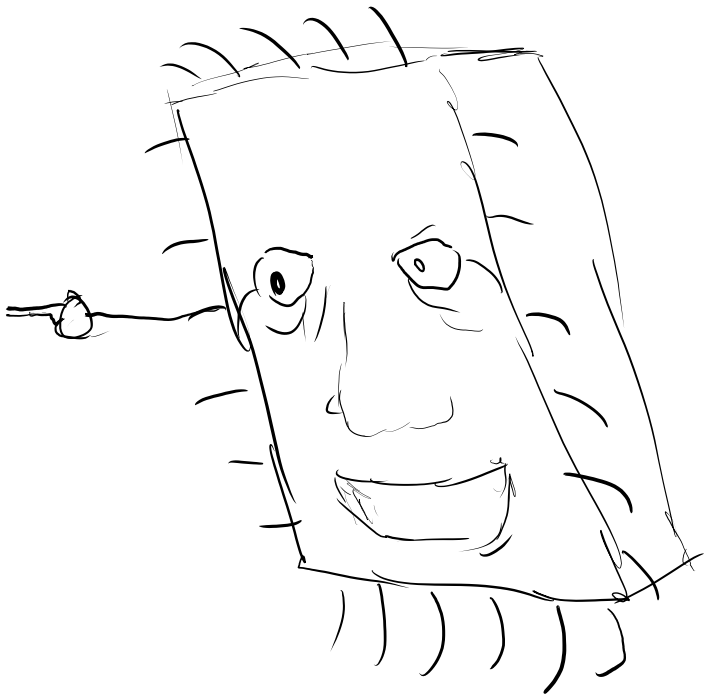
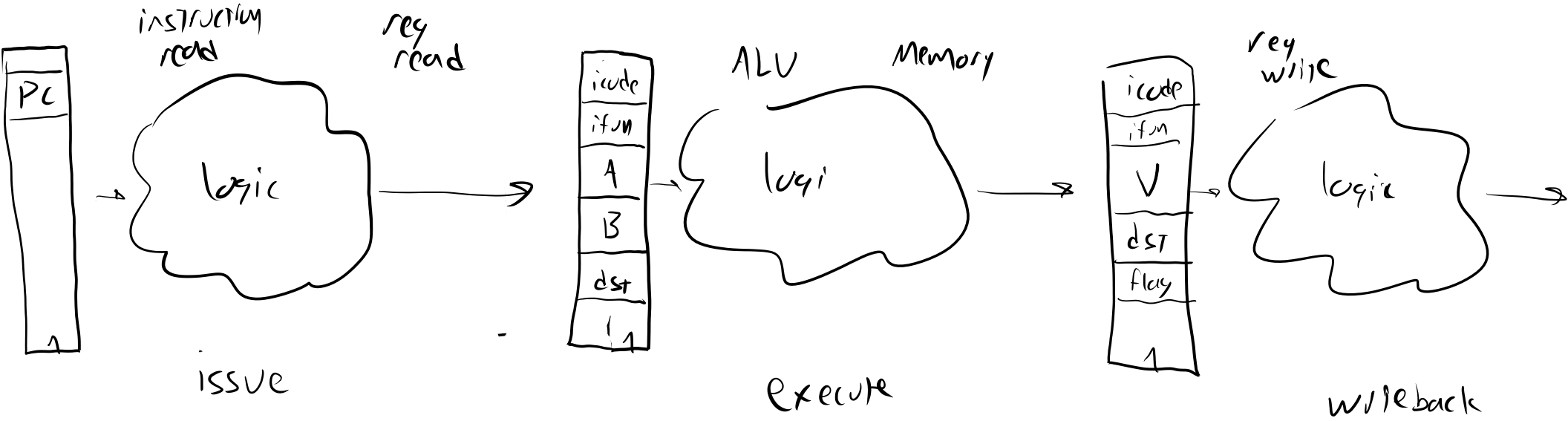
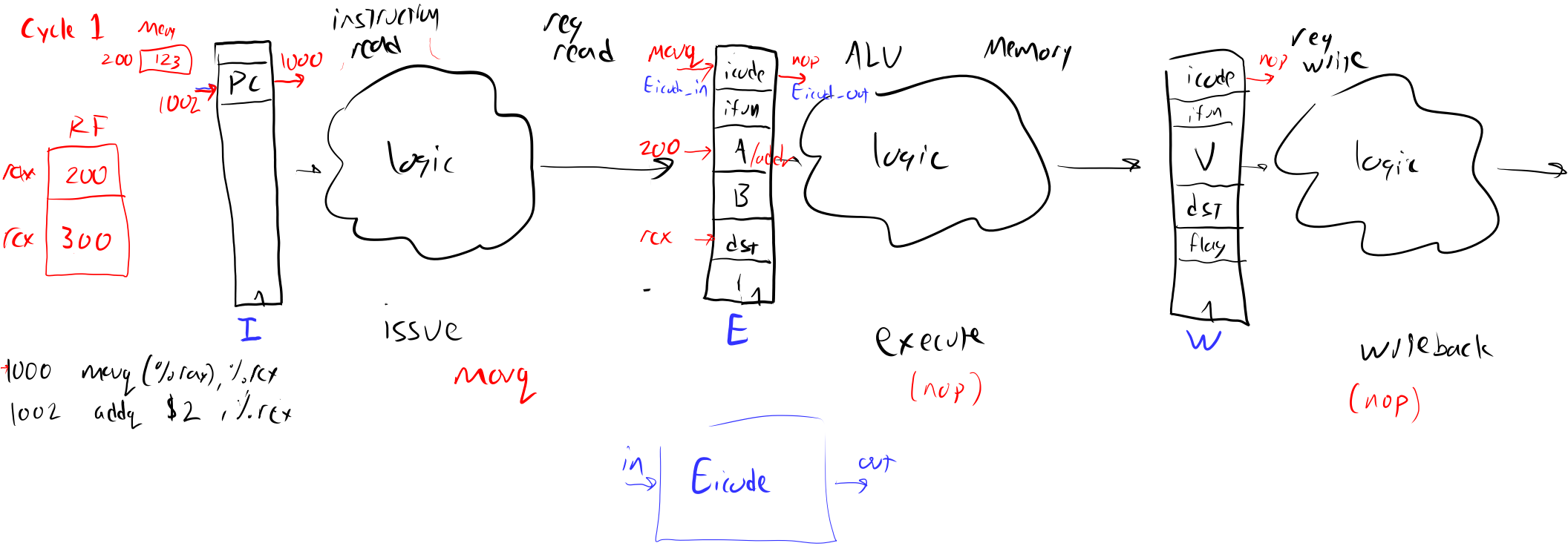
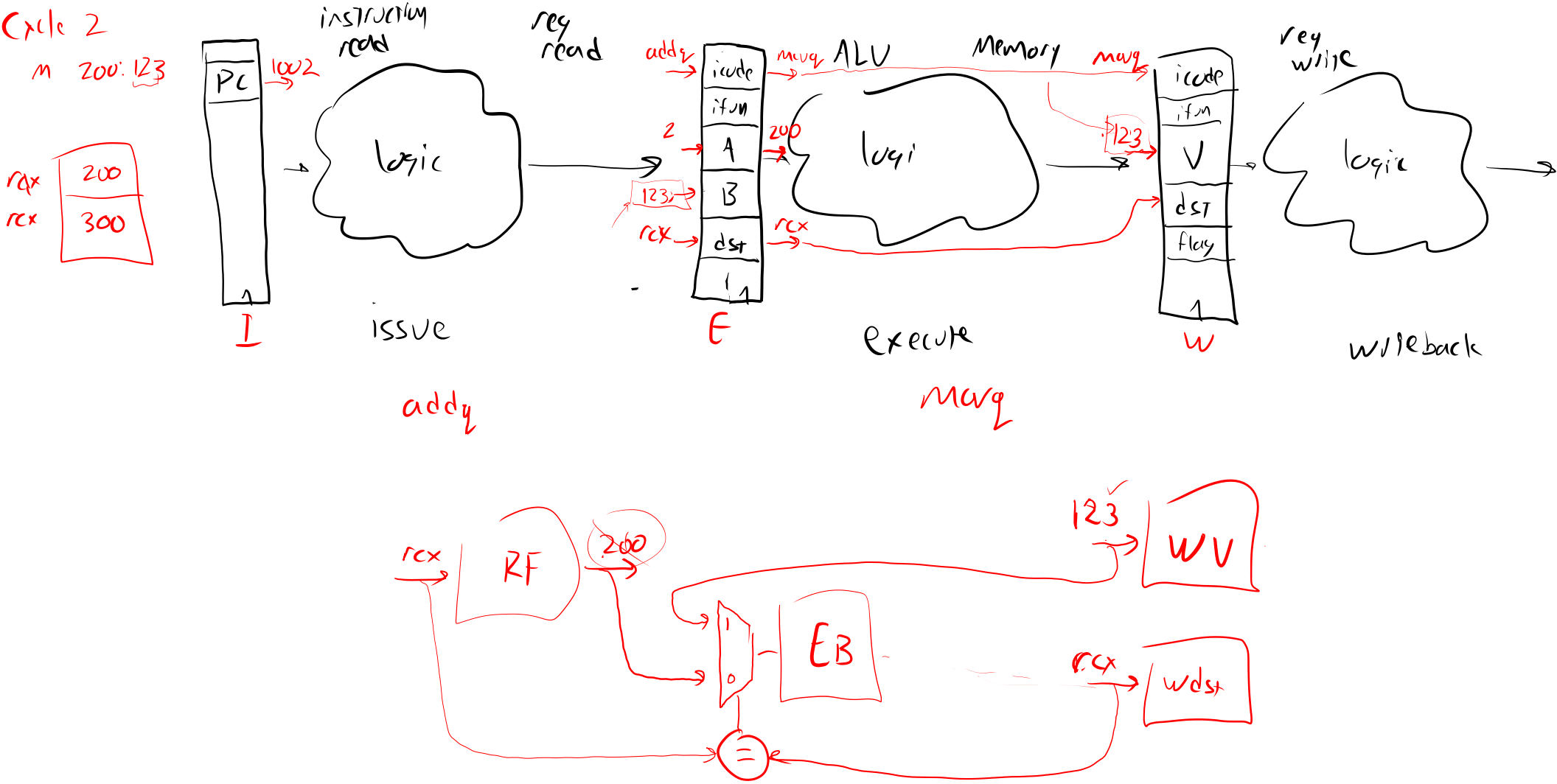

PIPELINE






instruction read
reg read
PC
logic
icode
ifun
A
B
dst
1
ALU
Memory
logi
V
reg write
issue
execute
writeback


Cycle 1
mem
200
123
PC
1000
1002
RF
rax
200
rcx
300
instruction read
logic
I
issue
movq
reg read
movq
icode
ifun
A
B
dst
I
rcx
E
nop
Ecode_in
Ecode_out
ALU
Memory
logic
execute
(nop)
icode
ifun
V
dst
flag
W
nop
reg write
logic
writeback
(nop)
1000 movq (%rax), %rcx
1002 addq $2, %rcx
in
Ecode
out

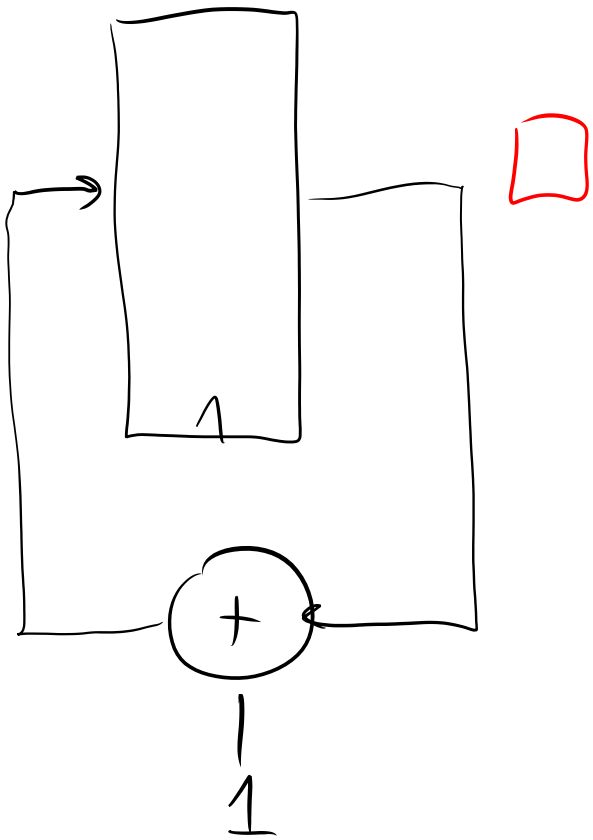

Cycle 2
M 200: 123
rax 200
rcx 300
PC
1002
instruction read
reg read
logic
I
issue
addq
2
123
rcx
icode
ifun
A
B
dst
valA
valB
E
ALU
Memory
mrmq
200
123
rcx
logic
execute
mrmq
icode
ifun
V
dst
flag
W
reg write
logic
writeback

rcx
RF
200
123
WV
1
0
EB
rcx
wdst
=

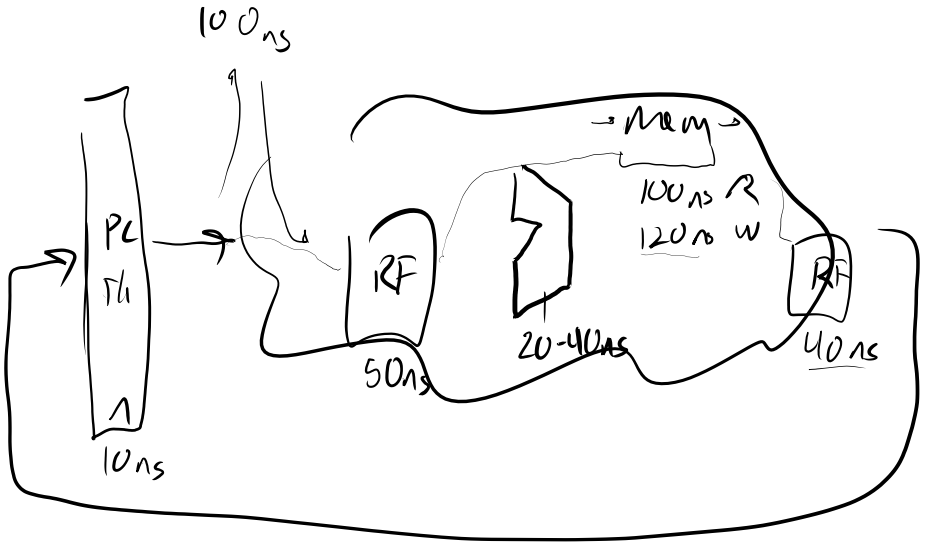
addq %rax, %rcx

addq %rax, %rcx

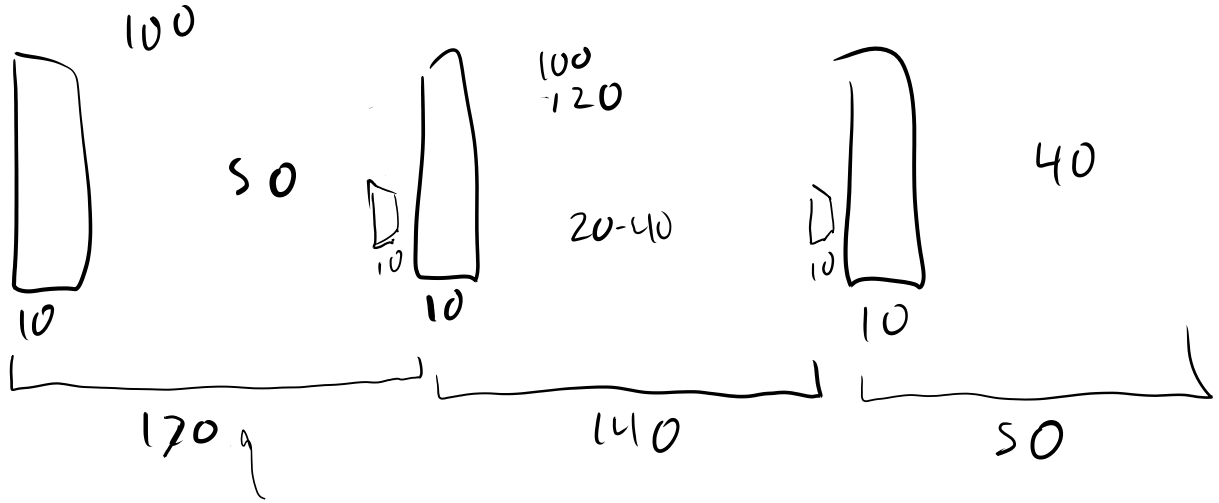
addq %rax, %rcx



timing clock speed : slowest for longest logic path



10 + 100 + 50 + 100 + 40 = 300ns



250 ns = 2.8MHz

= 170ns = 5.8MHz