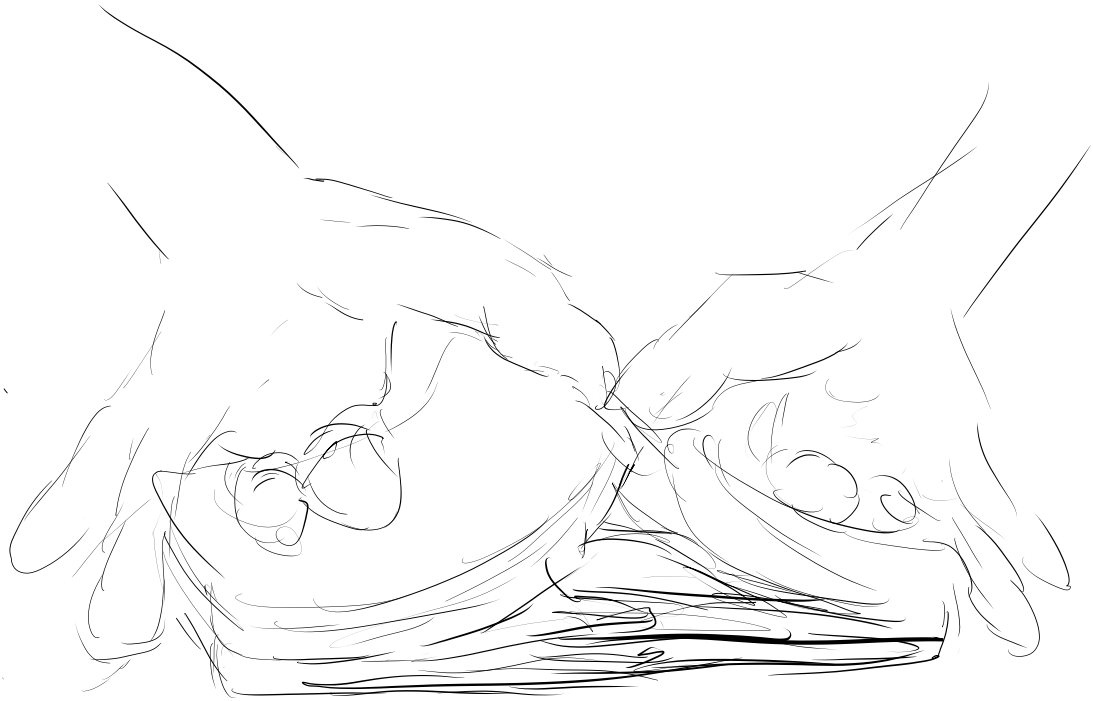
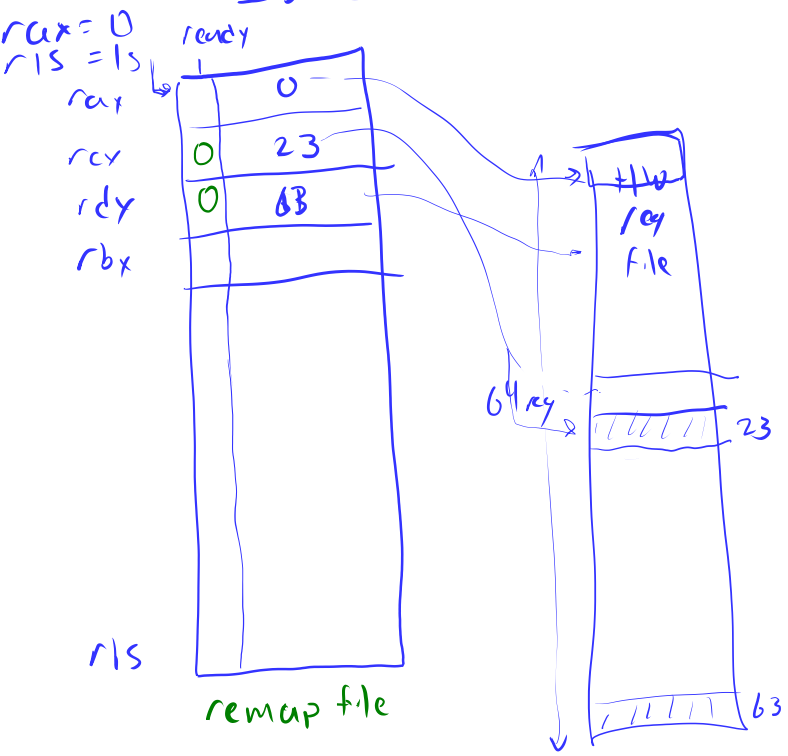


Each inst has unique dest reg

reg. renaming

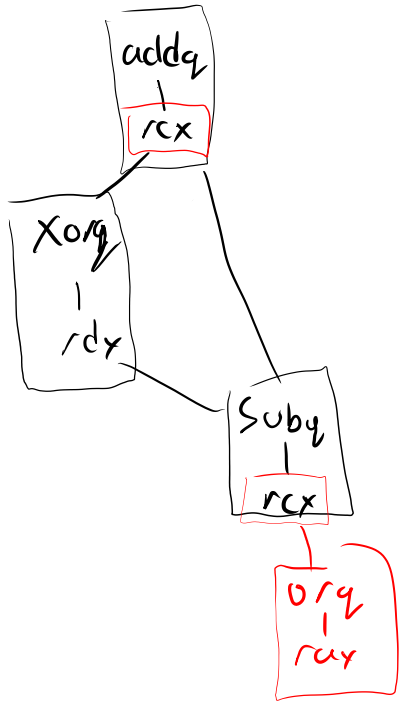


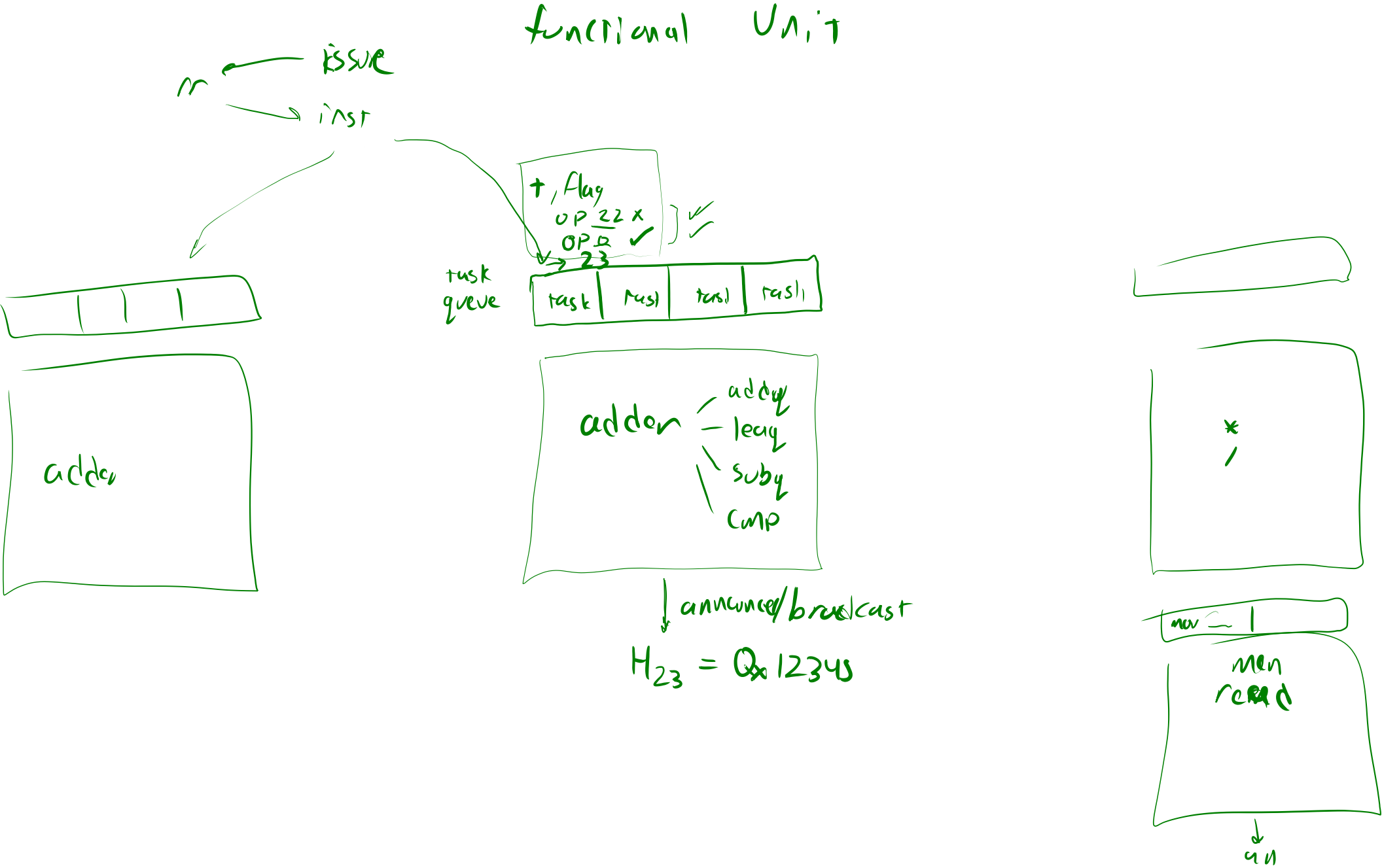
dependency Graph

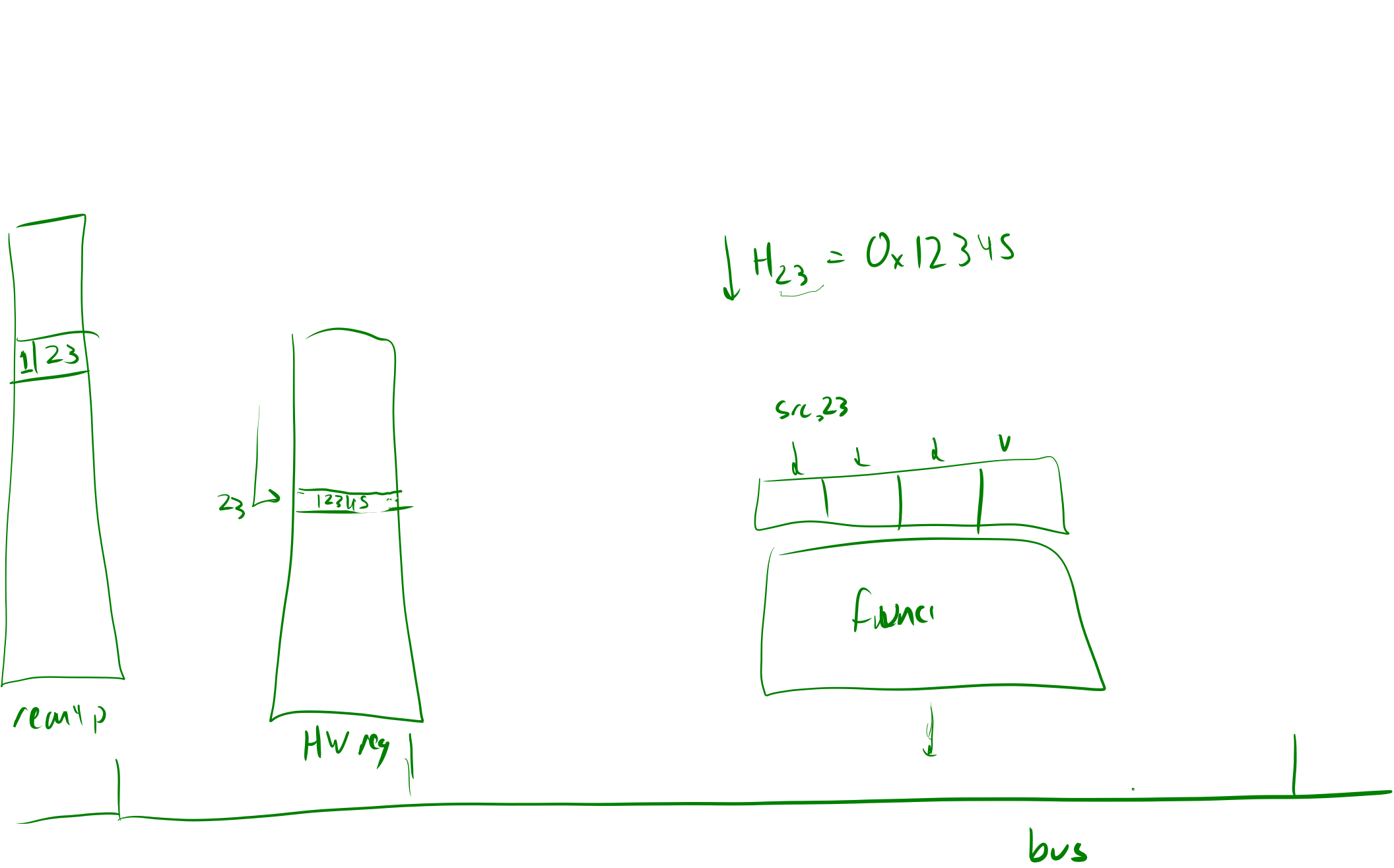
```
addq  %rax , %rcx
xorq  %rcx , %rdx
subq  %rdx , %rcx
orq   %rcx , %rax
```

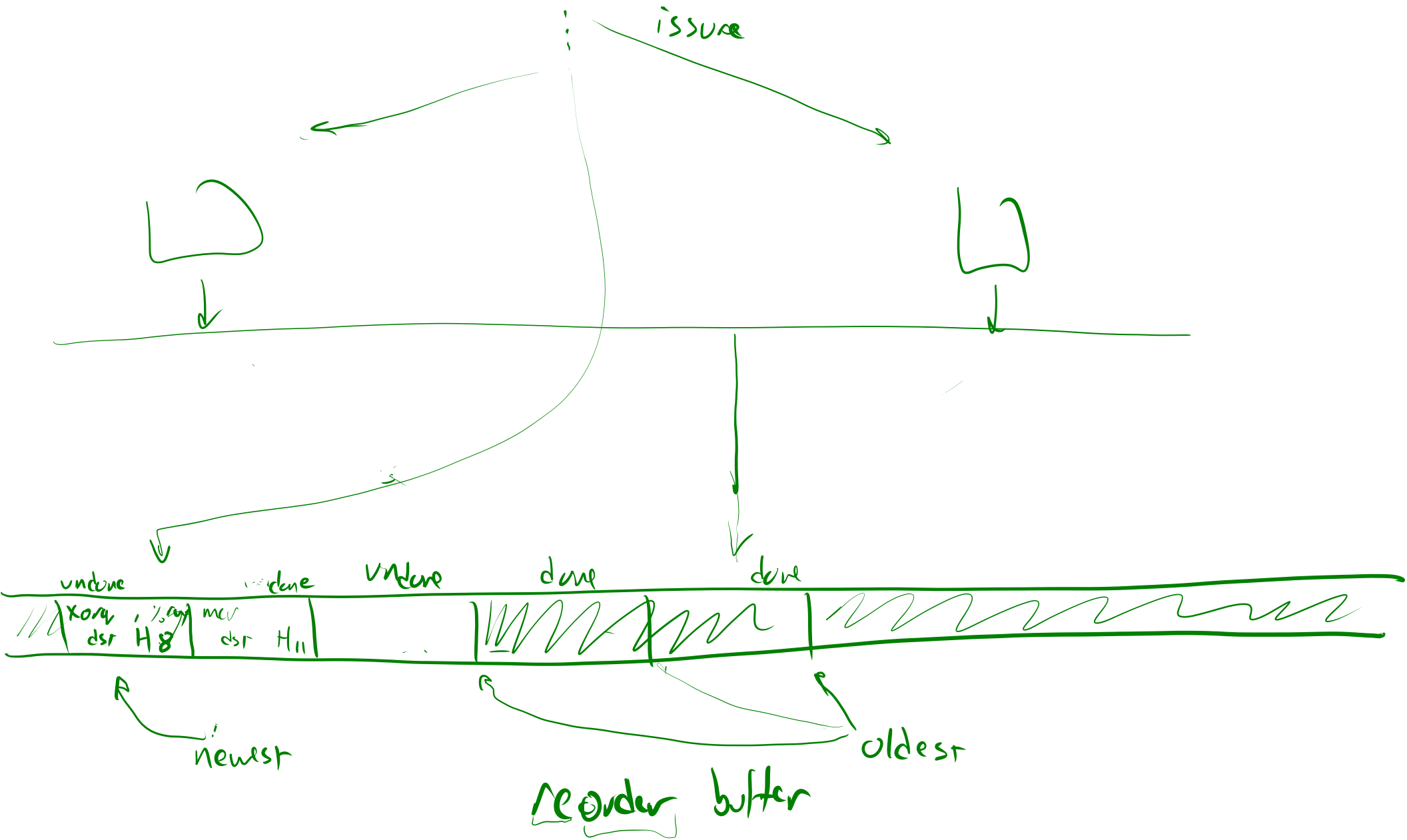
$\rightarrow H_{23} = H_0 + H_{22}$

$\rightarrow H_{63} = H_{23} \wedge H_{11}$



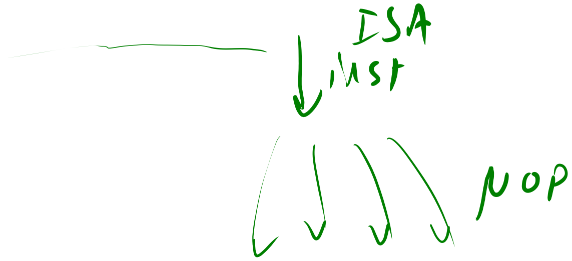

functional Unit
issue
inst
t, flag
OP 22 x
OP B ✓
23
task queue
task
task
task
task
adder
adder
addq
leaq
subq
cmp
announced/broadcast
H_{23} = 0x1234
*
/
mov — 1
mem read

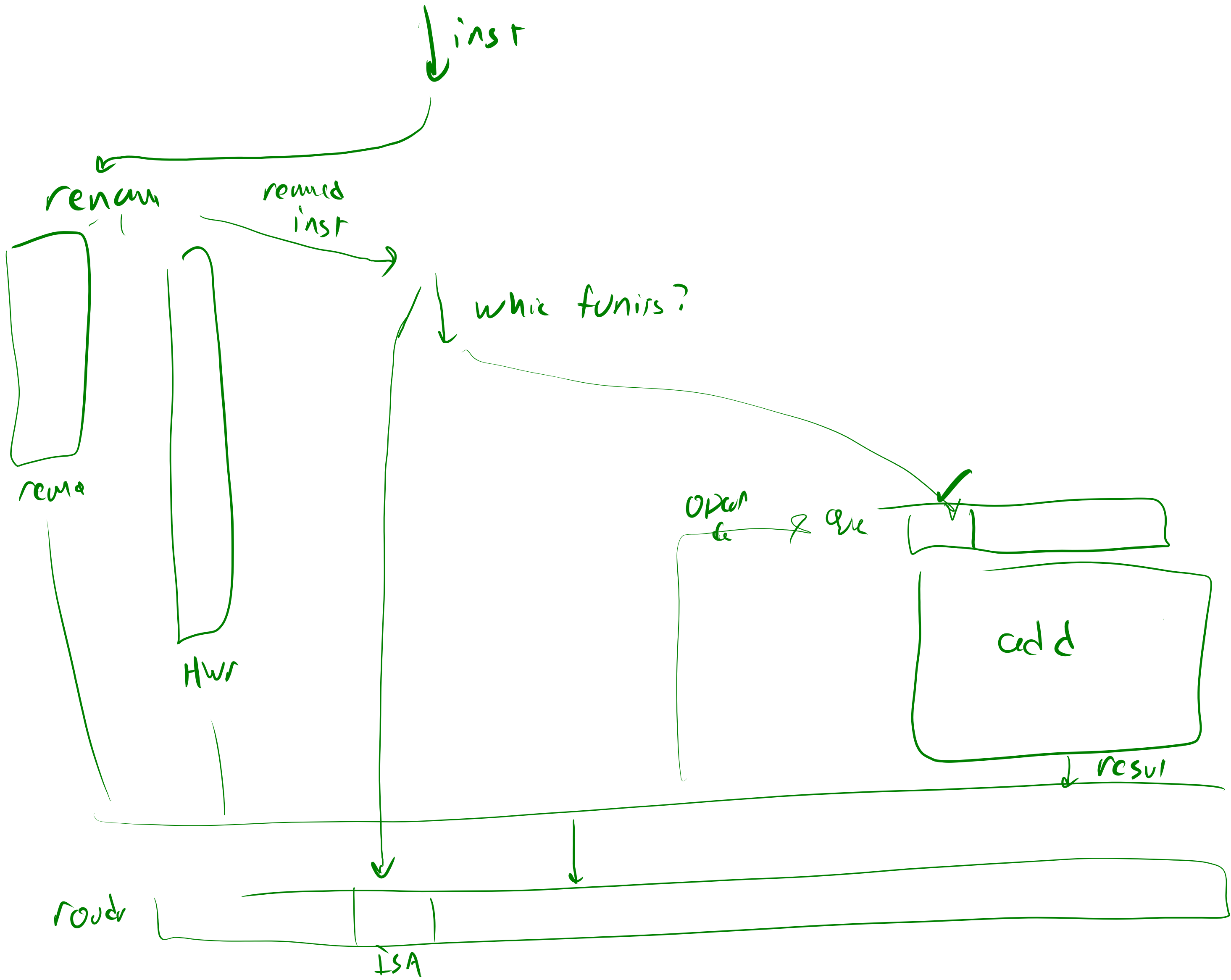

$H_{23} = 0x12345$
1 23
23
12345
src, 23
d
d
d
v
func
remap
HW reg
bus


issue
undone
done
done
newest
oldest
reorder buffer

CISC / RISC

x86 → ARM





N ops

ISA

% 10

AAA → Translum

+

(un