Morteza Baradaran

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Overview

My interests lie broadly in Computer Architecture, Domain Specific Accelerators, and Bioinformatics. I'm interested in exploring novel hardware and software techniques to enhance the performance, energy efficiency, and programmability of domain specific accelerators. I also have extensive experience in designing high-performance, energy-efficient embedded systems for core consumer products.

Education

University of Virginia, Charlottesville, USA — Sep. 2021 - Now
Ph.D., Computer Science (Advisor: Prof. Kevin Skadron) — (GPA: 3.95)

Sharif University of Technology, Tehran, Iran — Sep. 2010 - June 2012
M.Sc., Computer Architecture (Advisor: Prof. H. Sarbazi-Azad)

Shahed University, Tehran, Iran — Sep. 2006 - June 2010
B.Sc., Computer Engineering

Notable Projects

Accelerating Hybrid Transformer-CNN Models for Computer Vision through PIM (**Language:** *C/C++, Python*)
Goal: Accelerating hybrid Transformer-CNN models for computer vision using Processing-in-Memory.

PARMIK: PArtial Read Matching with Inexpensive K-mers (**Language:** *C/C++, Python*)
Goal: A fast and memory-efficient tool for identifying the "Partial Match" region between two genomic sequences.
Links: GitHub | Paper

PIMeval simulator and PIMbench suite (**Language:** *C/C++, Python*)
Goal: A PIM simulation and benchmark framework.
Links: GitHub | Paper

Swift: A Multi-FPGA Framework for Scaling Up Accelerated Graph Analytics (**Language:** *C/C++, Python*)
Goal: A scalable FPGA-based graph accelerator framework to handle large graphs efficiently.
Links: Paper

TriPIM: Efficient Triangle Counting on PIM Technologies — A Binary Search Approach (**Language:** *C/C++, Python*)
Goal: Efficient Triangle Counting Powered by Binary Search and In-Memory Processing (UPMEM).
Links: GitHub

ECG: Expressing Locality and Prefetching for Optimal Caching in Graph Structures (**Language:** *C/C++, Python*)
Goal: Enriching graph data with cache optimizations to improve prefetching and replacement policies in graph analytics.
Links: GitHub | Paper

HashMem: PIM-based Hashmap Accelerator (**Language:** *C/C++*)
Goal: A PIM-based Hashmap Accelerator.
Links: GitHub | Paper

Energy Consumption Analysis of Instruction Cache Prefetching (**Language:** *C/C++*, **Framework:** *ChampSim, CACTI-7*)
Goal: Evaluating the energy consumption of instruction cache prefetching techniques.
Links: GitHub | Paper

Banking Integrated Card Personalization System (IPS) (**Language:** *C/C++, Java*)
Goal: A Banking Card Personalization System Capable of Acquiring Customers' data and Personalizing it for Banking Cards.

Automatic Train Control Systems for Metro and Urban Railway (**Language:** *C++*)
Goal: Developing and Analyzing Metro & Urban Railway Signalling and Telecommunication Systems (i.e., ATC, ATP, etc).

Publications

- **M. Baradaran**, R. Layer, and K. Skadron, "PARMIK: PArtial Read Matching with Inexpensive K-mers," Genome Research, 2024. Submitted
- F. A. Siddique, D. Guo, Z. Fan, M. Gholamrezaei, **M. Baradaran**, A. Ahmed, H. Abbot, K. Durrer, K. Nandagopal, E. Ermovick, K. Kiyawat, B. Gul, A. Mughrabi, A. Venkat, and K. Skadron, "Architectural Modeling and Benchmarking for Digital DRAM PIM," in *International Symposium on Workload Characterization (IISWC)*, 2024
- W. Jaiyeoba, A. T. Mughrabi, **M. Baradaran**, B. Gul, and K. Skadron, "Swift: A Multi-FPGA Framework for Scaling Up Accelerated Graph Analytics," in *International Conference on Field Programmable Technology (FPT)*, 2024
- A. T. Mughrabi, **M. Baradaran**, A. Samara, and K. Skadron, "ECG: Expressing Locality and Prefetching for Optimal Caching in Graph Structures," in *International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*, 2024

- **M. Baradaran**, A. Ansari, M. Sadrosadati, and H. Sarbazi-Azad, "Energy Consumption Analysis of Instruction Cache Prefetching," in *International Symposium on Computer Architecture and High Performance Computing Workshops (SBAC-PADW)*, 2023
- A. Shekar, **M. Baradaran**, S. Tajdari, and K. Skadron, "HashMem: PIM-based Hashmap Accelerator," in *Fifth International Workshop on Domain-Specific System Architecture (DOSSA-5)*, 2023
- **M. Baradaran** and M. Zarei, "Theory of Automata and Machine Language," in *National Library of Iran, ISBN 978-600-6927-22-0, 2012-2013*

Presentations

TECHCON (presentation) Sep 2024
Title: TriPIM: Efficient Triangle Counting on PIM Technologies – A Binary Search Approach

Genome Informatics (poster) Dec 2023
Title: Enhancing pandemic preparedness–A novel partial matching approach for identifying similar genetic material from diverse sources for pathogen surveillance

Teaching Experience

Teaching Assistant, CS3130: Undergraduate Computer Systems & Organization 2 Fall 2024
University of Virginia

Teaching Assistant, CS4414: Undergraduate Operating System Fall 2023
University of Virginia

Teaching Assistant, CS4414: Undergraduate Operating System Fall 2022
University of Virginia

Skills

Programming Languages/APIs:
• C/C++, Java, Python, Bash, Assembly Programming (x86), Verilog

Simulators and Analyzers:
• Gem5, SniperSim, DRAMsim3, Multi2Sim, ChampSim, CACTI, Synopsys Design Compiler, UPMEM Functional Sim

Benchmarking and Performance Analysis:
• SPEC Benchmarks, PARSEC Benchmarks, GAP Benchmark Suite, prim-benchmarks, Gunrock, Ligra, InSituBench

Industry Software Skills:
• KEIL , Jet Brain (IntelliJ IDEA, Youtrack), Microsoft SQL Server, OOP, DevOps, Design Patterns, JUnit, Maven, Sonarqube

Practical Skills:
• Operating System, Large Language Models, Software Development, SOC Design, Embedded System Design

References

Three references will be made available upon request.