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# Temperature Aware Floorplanning

Yongkui Han, Israel Koren, C. Andras Moritz  
ARTS Lab, ECE Dept  
University of Massachusetts at Amherst

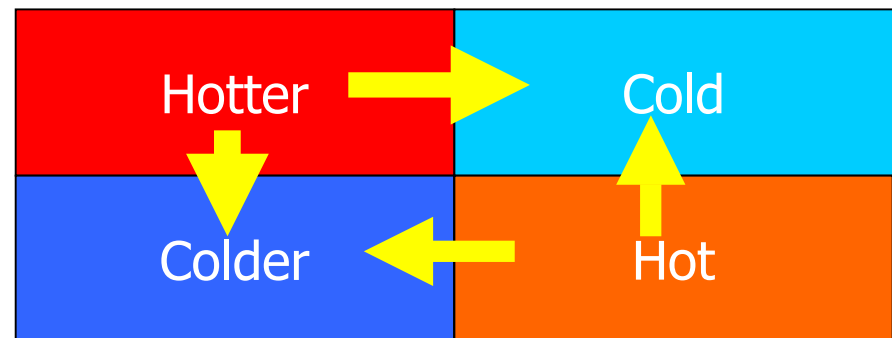
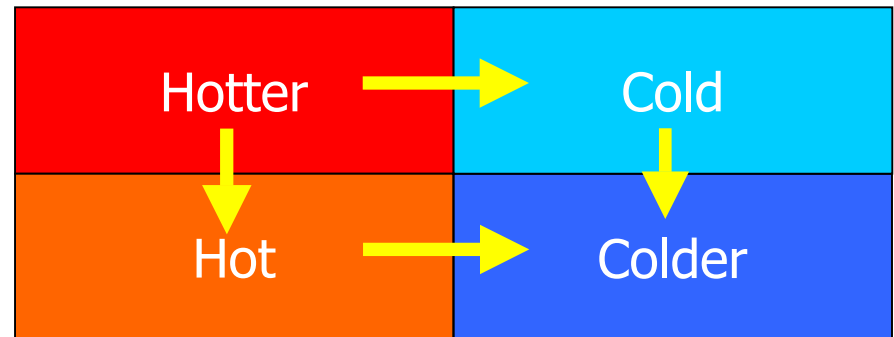


# Temperature Aware Design

- Temperature can affect
  - reliability
  - leakage power consumption
  - cost of cooling solutions
- Temperature not uniform across blocks
- Temperature of a block depends on its power density and that of adjacent blocks
- Placement of blocks (floorplan) can affect maximum temperature of chip

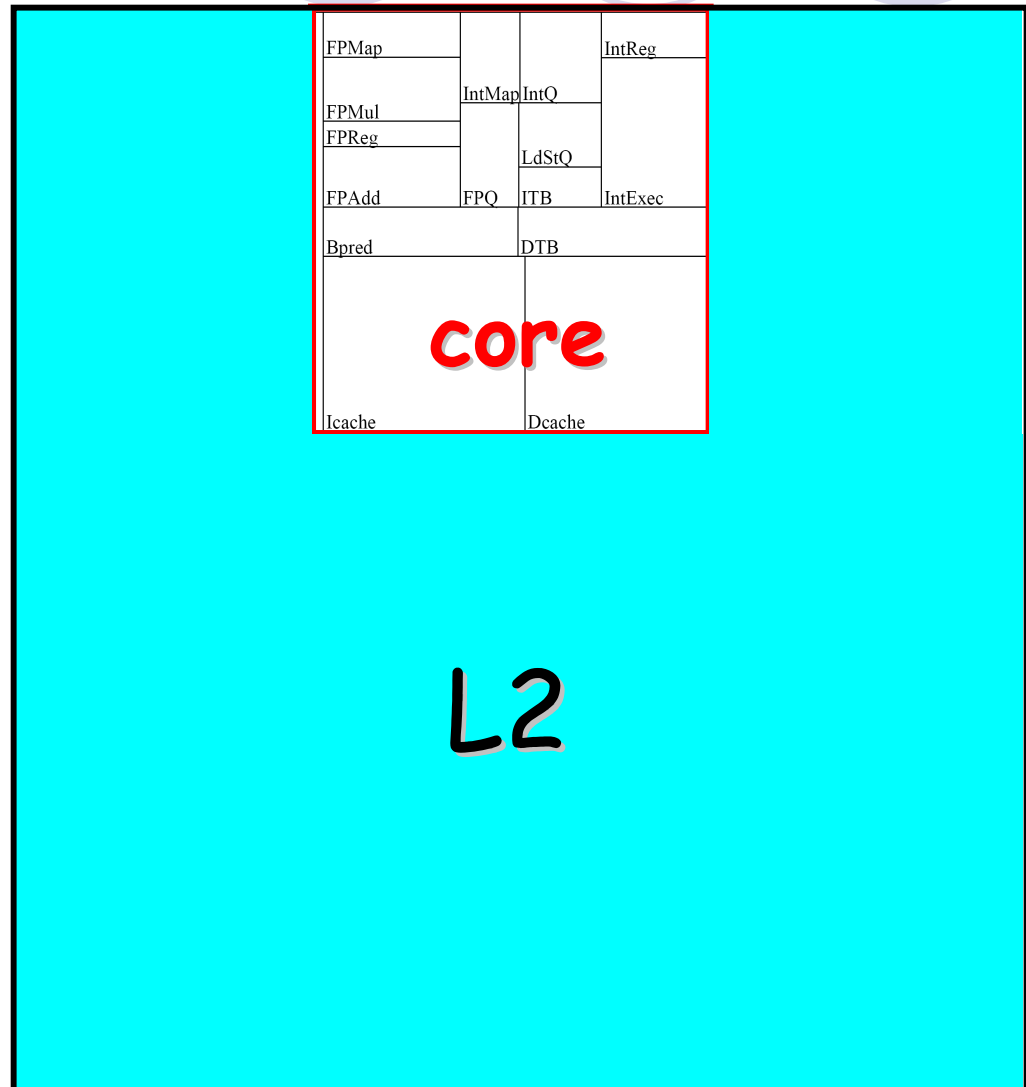
# Heat Diffusion Effects

- Heat diffusion between adjacent blocks
- The larger the temperature difference, the larger the heat diffusion
- Beneficial to place hot blocks adjacent to cold blocks



# Temperature Aware Floorplanning Example

Original Alpha 21364 floorplan



# Block Temperatures for *gcc* Benchmark

**L2cache=43°C**

<b>64.7°C</b> FPMap=64.7	IntMap=77.5		<b>120°C</b> IntReg=120.0
		IntQ=85.3	
FPMul=69.5	FPQ=78.0		
FPReg=73.5		LdStQ=96.9	
FPAdd=76.5		ITB=87.4	IntExec=100.2
Bpred=85.7		DTB=83.9	
Icache=79.9		Dcache=95.3	

**Steady-state temperature calculated using HotSpot 2.0 (UVa)**

# Rotated Floorplan

L2cache=43°C

Dcache=95.1	DTB=83.4	IntExec=97.4	ITB=86.0		IntQ=77.5
			LdStQ=94.1		
Icache=82.9	Bpred=89.1	FPQ=77.8		IntMap=72.3	
		FPAdd=80.1	FPReg=76.1	FPMul=70.4	FPMap=62.5
				IntReg=103.1	<b>103.1°C</b>

Reduction in MaxTemp: 16.9°C

# Manually Generated Floorplan

Reduction in  
MaxTemp: 21.8°C

Spread of  
Temperature:  
28.2°C vs 55.3°C

ITB=84.7	<b>98.2°C</b>			
	Bpred=98.2			
	FPMul=87.2	Icache=81.6		
	DTB=82.0		FPAdd=75.0	<b>70.0°C</b>
Dcache=94.7				
FPQ=83.6		IntExec=91.9		IntQ=70.0
		IntMap=80.8	FMap=74.3	
IntReg=98.0		FPrege=76.2		LdStQ=83.2



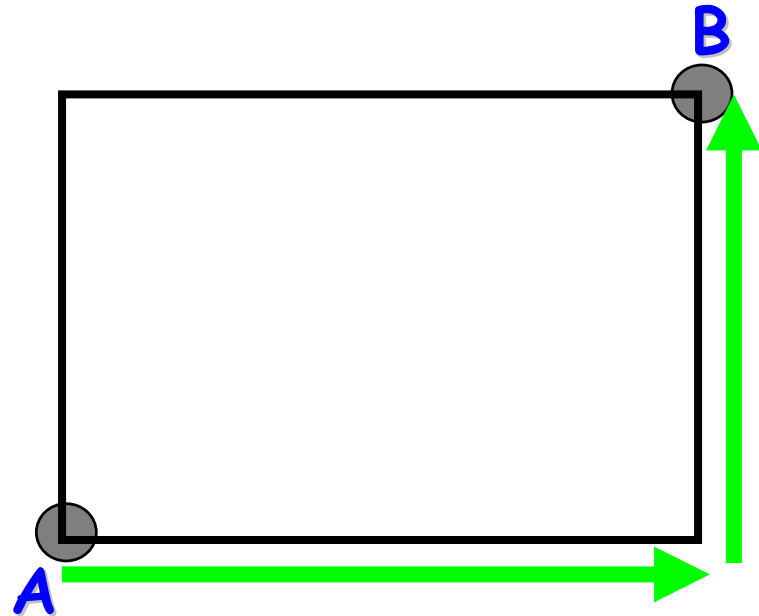
# Chip Performance?

- These new floorplans can reduce the maximum temperature on chip
- Issues:
  - How will these new floorplans affect chip performance?
  - If they compromise performance, can we find a floorplan which has both low maximum temperature and good performance?
  - What tradeoffs can we do in floorplanning?



# Metric of Chip Performance: Wire Length

- Wire length is a commonly used metric of chip performance
- HPWL (Half Perimeter Wire Length) is widely used in many floorplanning tools
- Critical paths are assigned larger weights



$$TotalWireLength = \sum W_{ij} * L_{ij}$$

# Temperature Aware Floorplanning

- Parquet 2.0 floorplanning tool (UMich)
- Objective of Parquet:  
Minimize a linear combination of chip area and total wire length (using simulated annealing)  
$$C_a * A + C_w * W$$
- Added temperature to objective function:  
$$C_a * A + C_w * W + C_t * T$$
  - $A$  - chip area,  $W$  - wire length,  $T$  - maximum temperature
  - We can adjust coefficients to achieve different optimization goals
- SPEC2000 benchmarks
  - Gcc as a representative benchmark

# Approximation for the Temperature

- **Heat Diffusion**

$$H(d1, d2) = (d1 - d2) * \textit{shared\_length}$$

- **$d_i$  - power density of block  $i$**

$$H(d) = \Sigma H(d, d_i)$$

$$D = \Sigma H(d), \text{ for all } \textit{possibly-hot} \text{ blocks}$$

# Modified Floorplan: Low-temp

Low maximum temperature

Reduction in MaxTemp:  
24.8°C

Increase in Wirelength:  
38.15%

$C_a = .4$ ,  $C_w = 0$ ,  $C_t = .6$

Smaller spread of  
temperature: 19.6°C

Unacceptable wire length

ITB=77.0	FPreG=82.8	IntMap=85.4	
			FPMul=75.9
	FPAdd=89.6	IntExec=95.2	
Dcache=94.4		FMap=82.4	
			Icache=80.4
DTB=75.8		Bpred=87.3	
			FPQ=80.3
LdStQ=84.4		IntQ=75.6	IntReg=94.9

**95.2°C**

**75.6°C**

# Modified Floorplan: Wire-temp

Short wirelength & low maximum temperature

Reduction in MaxTemp:  
21.1°C

Increase in Wirelength:  
0.67%

$C_a = .3$ ,  $C_w = .4$ ,  $C_t = .3$

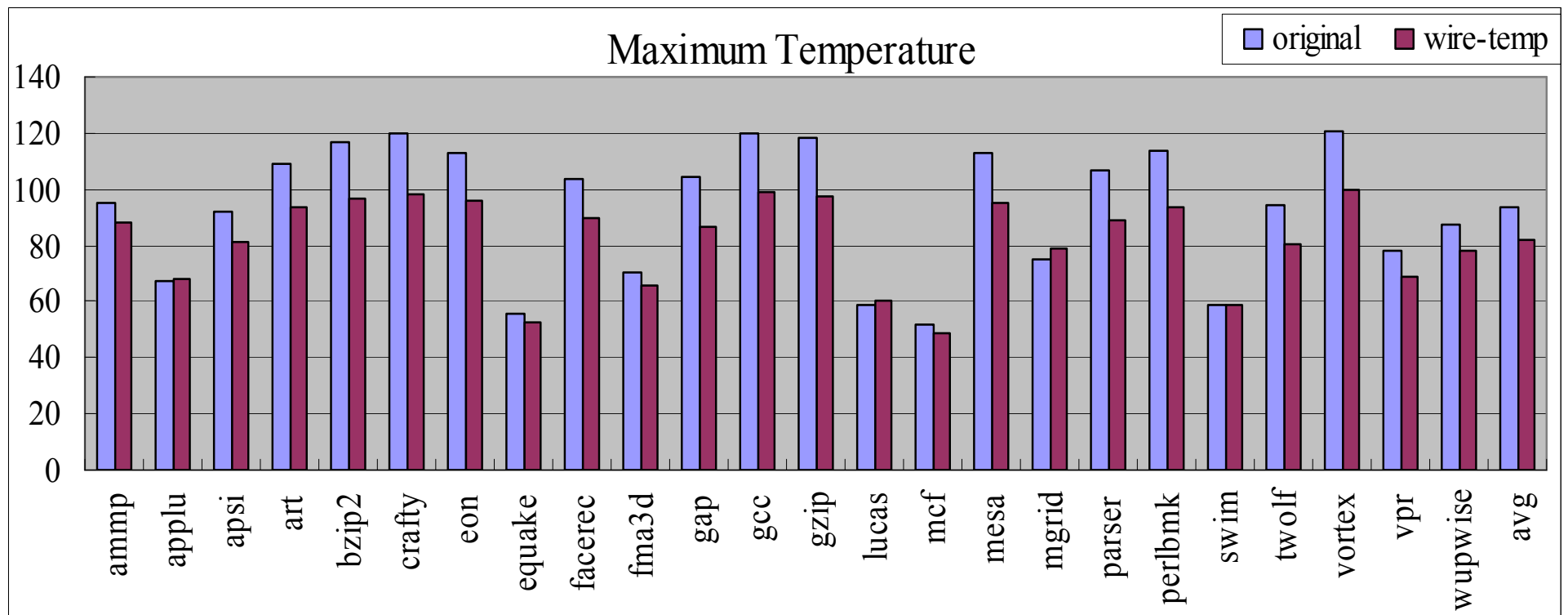
Small spread of temperature: 19.9°C

DTB=69.0		IntExec=94.8	
FPMul=84.4	FPAdd=85.8	FMap=83.2	
	FPReg=86.4	<b>98.9°C</b>	
	IntQ=86.3	IntReg=98.9	
	LdStQ=94.7		
	ITB=90.7	FPQ=79.4	
	Bpred=91.4	<b>79.0°C</b>	
	IntMap=79.0		
Dcache=89.3	Icache=80.1		

# Temperature Reductions for SPEC2000 Benchmarks

Average MaxTemp reduction: **12°C**

For many benchmarks, reductions are larger than **20°C**



# Modified Floorplan: Short-wire

Short wire length

Increase in MaxTemp:  
0.1°C

Reduction in Wirelength:  
4.07%

Ca=.4, Cw=.6, Ct=0

MaxTemp almost  
unchanged

FPMul=69.7 <b>69.7°C</b>	FPAdd=74.7	FPMMap=76.0	<b>120.1°C</b> IntReg=120.1
		FPReg=79.3	
		FPQ=80.6	IntExec=101.2
		LdStQ=90.4	
		ITB=85.1	
Icache=82.2		IntQ=81.0	
		IntMap=76.9	
		DTB=72.3	
Bpred=85.9	Dcache=91.7		

# Modified Floorplan: High-temp

High maximum temperature

MaxTemp increase:  
12.3°C

Wirelength increase:  
6.36%

Ca=.4, Cw=0, Ct=-.6

High MaxTemp

	IntReg=132.0	<b>132°C</b>
	LdStQ=119.8	
	FPReg=103.6	
IntExec=100.2		
IntMap=84.0	FPMul=88.6	
IntQ=73.4	DTB=75.1	
ITB=76.5		
	FPQ=71.7	
Bpred=83.1	FMap=71.8	
Icache=75.7		<b>70.3°C</b>
		FPAdd=70.3



# Summary - Alpha

Floorplan	Area ( $mm^2$ )	Increase	Wire length ( $m$ )	Increase	Temp ( $^{\circ}C$ )	Reduction ( $^{\circ}C$ )
Original	253.1	0%	17.93	0%	120.0	0
Manual	253.1	0%	23.21	29.45%	98.2	21.8
Rotated	253.1	0%	18.32	2.18%	103.1	16.1
Low-temp	254.1	0.4%	24.77	38.15%	95.2	24.8
Wire-temp	255.1	0.8%	18.05	0.67%	98.9	21.1
Short-wire	256.3	0.9%	17.20	-4.07%	120.1	-0.1
High-temp	255.1	0.8%	19.07	6.36%	132.3	-12.3

# Pentium Pro

Original floorplan

**74.0°C**

BIUL=74.0	BIUR=75.3	AGU=81.2	
		Int=100.0	
		MOB=87.5	FP=86.6
Dcache=83.6	BIUB=76.3	RS=83.0	
BLK=77.9			
Branch=85.0		RAT=84.0	ROB=89.0
IFetch=86.5	IDecode=86.8		Micro=80.5

**100°C**

Reduction in MaxTemp: 6.3°C  
Increase in Wirelength: 13%

Low maximum temperature

**75.0°C**

		BLK=78.5	
		Int=93.7	
IFetch=86.3		AGU=82.8	BIUB=75.0
	BIUL=76.9		
	Branch=83.3	BIUR=77.8	
RS=81.6			FP=83.9
		ROB=88.5	
		MOB=87.7	
Dcache=86.5	RAT=83.8	Micro=82.0	IDecode=87.5

**93.7°C**

Floorplan with highest maximum temperature **110.5°C**

Smaller improvement due to smaller spread of temperature in Pentium Pro: 26°C vs 55°C in Alpha



# Conclusions

- Our observations:
  - Maximum temperature reduction of **21°C** while keeping a comparable wire length for Alpha processor
  - **6.3°C** reduction in maximum temperature for Pentium Pro with a penalty of 13% in wire length
- Temperature-aware floorplanning can greatly improve temperature distribution of a chip