A Preliminary Evaluation on Energy Efficiency of a Temperature-aware Multicore-processor

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Outline

- Background
- Contrail processor architecture
- Temperature awareness
  - Active power reduction
  - Leakage power management
- Evaluation
- Conclusion

Background

- High-performance embedded processors are required by smart mobile devices
  - 3D video game, digital camera, digital video, MP3 player … on cell phones
- Power consumption is also increased
- Multicore-processors is one of solutions
  - Temperature due to large leakage is a problem

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Contrail processors

- Program is divided into 2 types of streams
  - Each stream is executed quasi-independently on a multicore processor
- Speculation stream:
  - Main part of the program
  - Some instructions are removed via speculation
- Verification streams:
  - Verification of every speculation
  - Verification shouldn't be fast and can be cool

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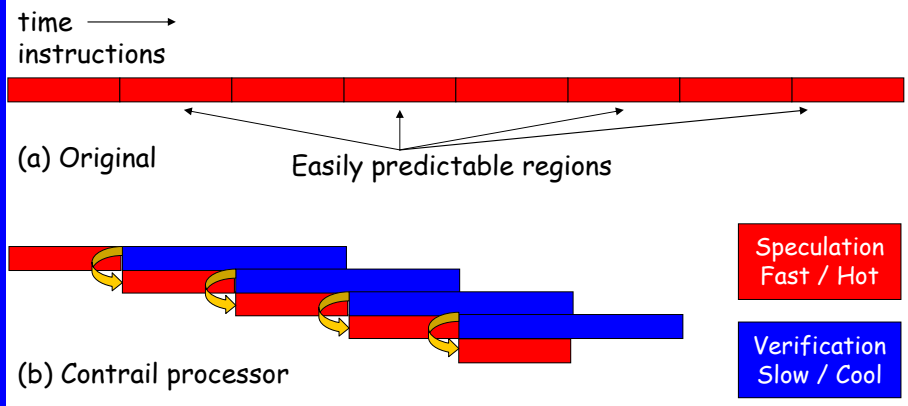
Execution example



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Temperature awareness

- Hot core rotation
- Power reduction
  - Active power reduction
  - Leakage power management

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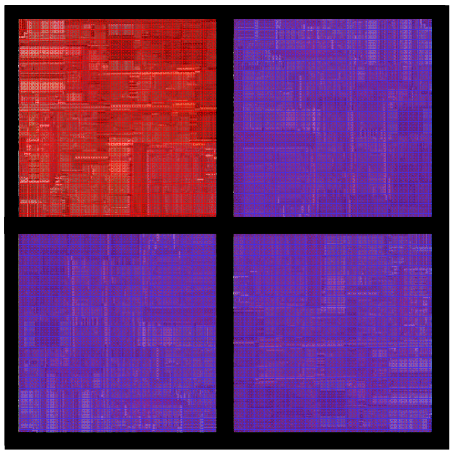
Hot core rotation



Speculation
Hot

Verification
Cool

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Active power reduction

- Assumption
  - V & f for verification = 1/2x V & f for speculation
  - Speculation : verification = 1 : 1
- Results
  - Speculation
  - Verificat

37.5%
Energy reduction

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Leakage power management

- Leakage might be increased
  - Contrail processor has multiple cores
- Key observation
  - Only one core has to be fast
- Leakage management
  - Power supply reduction & cut
  - Reverse body bias to raise V_{th}

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Evaluation

- 4-core Contrail processor vs. single-core
  - 2-way OoO superscalar base & cores
    - Ideal caches
    - Perfect branch prediction
    - Perfect memory disambiguation
  - 2K-entry last-value predictor
  - Fixed interval partitioning: 32 instructions
- MASE / SimpleScalar / PISA tool set
- MiBench
  - CRC, FFT, and StringSearch

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Assumptions on power

- DVS is based on SAMSUN's ARM
  - (1.2GHz @1.1V) <-> (600MHz @0.7V)
- Leakage power = active power
  - Temperature = 100°C
- Reverse body bias reduces leakage by 2x
- Leakage of idle cores is zero

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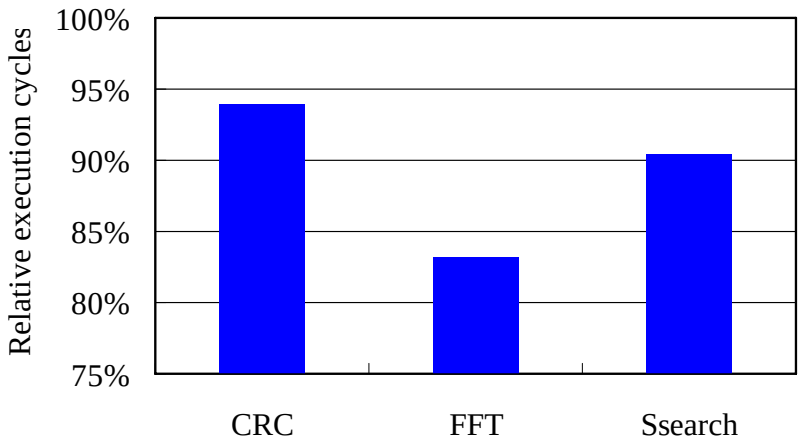
Relative execution cycles



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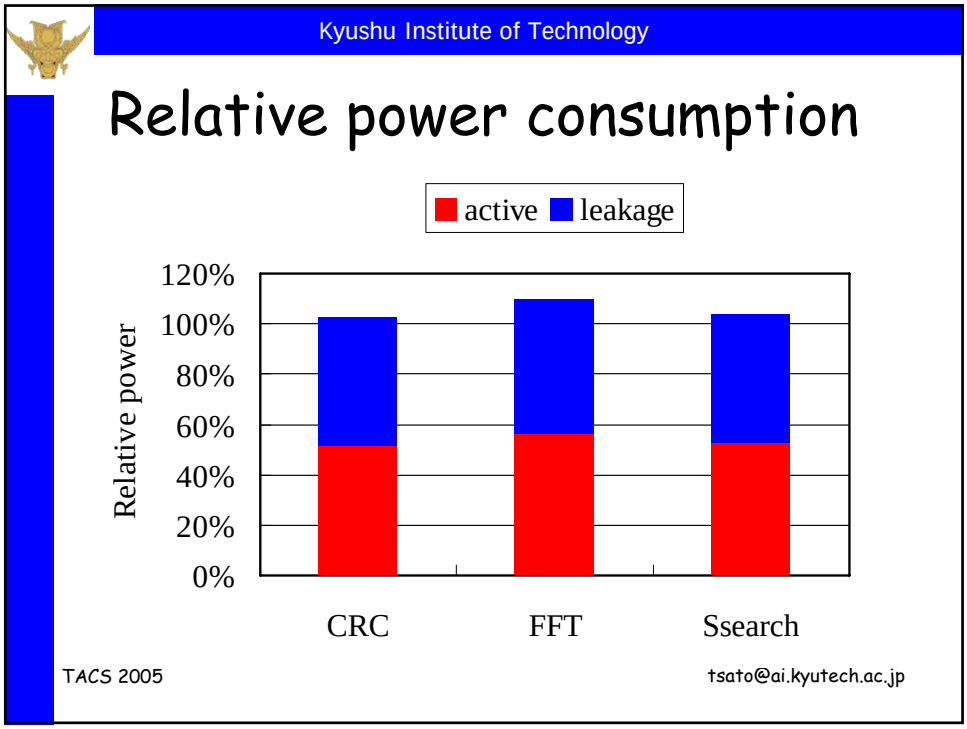
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Relative power consumption
active
leakage
120%
100%
80%
60%
40%
20%
0%
Relative power
CRC
FFT
Ssearch
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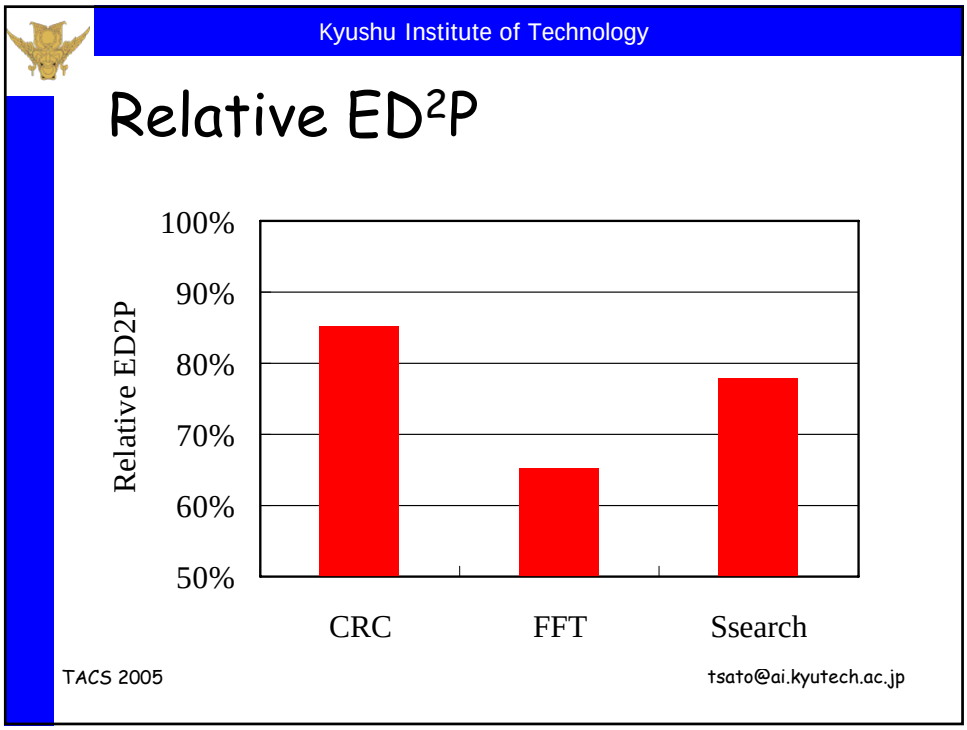
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Relative ED²P
100%
90%
80%
70%
60%
50%
Relative ED2P
CRC
FFT
Ssearch
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Conclusion

- We proposed a temperature-aware multicore-processor, Contrail processors
- Temperature would be reduced by
  - Hot core rotation
  - Active power reduction
  - Leakage power management
- Simulations showed 25% ED^2P reduction

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